Wistron Confidential

MV

2008/05/15 REV :-1

<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Karia*

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KARIA DESCRETE BLOCK DIAGRAM

Project code : 91.4V901.001
PCB P/N :
Revision : MV

SYSTEM DC/DC SC471AML	
INPUTS	OUTPUTS
B+	VGA_CORE 45

SYSTEM DC/DC TPS5116	
INPUTS	OUTPUTS
B+	+1.8V 7A 47 +0.9V 1A

SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
B+	+5VALW 7A +3VALW 6A 46

SYSTEM DC/DC SC412A	
INPUTS	OUTPUTS
B+	+1.5VS 3A 50 +1.05VM 13A 48

CHARGER BQ27470	
INPUTS	OUTPUTS
BATT_A BATT_B	BATT 18V 3.0A 5V 100mA 51

CPU DC/DC ISL6260A	
INPUTS	OUTPUTS
B+	+VCC_CORE 0.844~1.3V 44A 43

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	GND
L6:	VCC
L7:	Signal 4
L8:	Signal 5
L9:	GND
L10:	Signal 6

CLK GEN
SLG8SP553 16

Intel CPU
Penryn 5,6,7

HOST BUS
FSB 667/800/1067MHz

VRAM 0 58
VRAM 1 58
GDDR 3

DDRII 800 Slot 0 14
DDRII 800 Slot 1 15
DDRII 667/800 Channel A
DDR II 667/800 Channel B

Cantiga PM
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
8,9,10,11,12,13

PCIE x 16

ATI
M82-SCE
52,53,54,55,56,57

RGB CRT
LVDS
CRT 17
LCD 18

Smart Card ISO7816 37
1394 37
SD/MMC 37
Ricoh 5C835
CardReader
36,37
PCI

DMI x4
Controller link 0

INTEL
ICH9-M
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
Serial Peripheral I/F
ACPI 1.1
LPC I/F
4 SATA
PCI/PCI BRIDGE
19,20,21,22,23

SMBus
Thermal Sensor EMC2103 39
Accelerometer LIS302DLTR 24

Fingerprinter AES2810B 38
CAMERA 38
Blue Tooth
USB x 3 28
HDD Cnn SATA 24
ODD Cnn 24
USB 2.0
SATA
SATA

RJ45 CONN 26
Intel Ninevah-MM (BOAZ) 10/100/1000 25
GLCI

RJ11 CONN 31
MODEM MDC V1.5 31
HD Audio

AUDIO CODEC
ADI 1984A

INTERNAL MIC
MIC IN
Headphone
PRE-AMP TLV2462

SPEAKER
OP AMP TI 6041A

LPC Bus
SPI

KBC
SMSC KBC1091 30
TPM SLB9635TT 29
SMSC Super I/O LPC47N217 40

PCIE+USB 2.0
C-LINK
PCIE x 2

TI2231
Express Card 54
Mini-Card*2 802.11abg/n WWAN 27

SPI
Flash ROM 32Mb x 1(AMT) 29
Tauch Pad 31
Int. KB 31
Capacitive Button 38

DOCK
PCIE*2 PS2 SATA*1 USB*2 Serial Port Parallel Port LINE IN/Out RJ45/RJ11 VGA DVI-D

<Variant Name>

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Discrete PV
03/11/08:
- Page 51 - Change R118 to 287K ohm from Vox information.
- Page 43 - Change R582.2 to +3VALW from +3VS to power U89.39 (3V3)
- Page 45 - Change R232 to NO INSTALL
- Page 30 - Remove D48, connect signal directly to ADP_PRES, and uninstall R558
- Page 27 - Reserve a 1u 0603 cap (NO INSTALL) on MC2_DISALBE (same as MC1_DISABLE)
- Page 19 - Add a 0 ohm series on PLT_RST# at U113.4
- Page 33 - Add a 0 ohm series on PM_PWROK_R at R175.2
- Page 13 - Uninstall BGA_CRACK circuit: U115, U116, R740, R744, R801, & R802
- Page 23 - Uninstall BGA_CRACK circuit: U117, U118, R803, R804, R805, & R806
- Page 39 - Change R710 (SHDN_SEL) to 15K 1% to use Internal Diode for H/W critical shutdown
- Page 57 - Add a discharging FET (gate connect to Q15.D) on 3.3V_DELAY at Q42.D
- Page 25 - May require a discharging FET for +3VM_LAN at Q39.D
- Page 32 - May need to change RGB q-switches power to +5VALW or +5VS (depending on wavy impact)
- Page 51 - Change R97 to 33K from 1.27K
- Page 41 - Change DAUGTH1 pin 52 and pin 54 to +5VS from +5VALW
- Page 41 - Remove ICH_SMB_CLK/DATA from DAUGTH1 pin 32 and 34

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Title: ***Change Notes List***

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Voltage Rails

o MEANS ON x MEANS OFF

State \ power plane	+BB LDO3 LDO5	+3VALW +5VALW	+1.8V +5V +0.9V	+5VS +3VS +1.8VS +1.5VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	O	O
S5 S4/Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader&1394	AD25	2	G,E

PCIE Devices

DEVICE	NUMBER	CHANNEL
UWB(no support)	1	1
WLAN	1	2
EXPRESS CARD	1	3
WWLAN	1	4
DOCKING	1	5
GIGA LAN	1	6

USB PORT	Device
0	USB1
1	Free
2	EX-P
3	WLAN
4	USB2
5	USB3
6	BLUETOOTH
7	WWAN
8	FignerPrint
9	Dock1
10	WEBCAM
11	DOCK2

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything
1U16V2ZY-2GP	Caps 1U ,Size 0402 Y5V
2D2U6D3V3MX	Caps 2.2U ,Size 0603 X5R

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	~~Floppy~~
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH9 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH9 Family) PCI Express Root Port -27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH9 Family) USB Universal Host Control
18	Intel 82801H (ICH9 Family) USB Universal Host Control Richo R5C835 Integrates FlashMedia Control Richo R5C835 Gemcore based SmartCard Control
19	Intel 82801H (ICH9 Family) PCI Express Root Port -27D6 Intel 82801H (ICH9 Family) USB Universal Host Control
20	Intel 82801H (ICH9 Family) USB Universal Host Control Intel 82801H (ICH9 Family) USB2 Enhanced Host Control
21	Intel 82801H (ICH9 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control
23	HP Mobile Data Protection Sensor

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Title: Karia List

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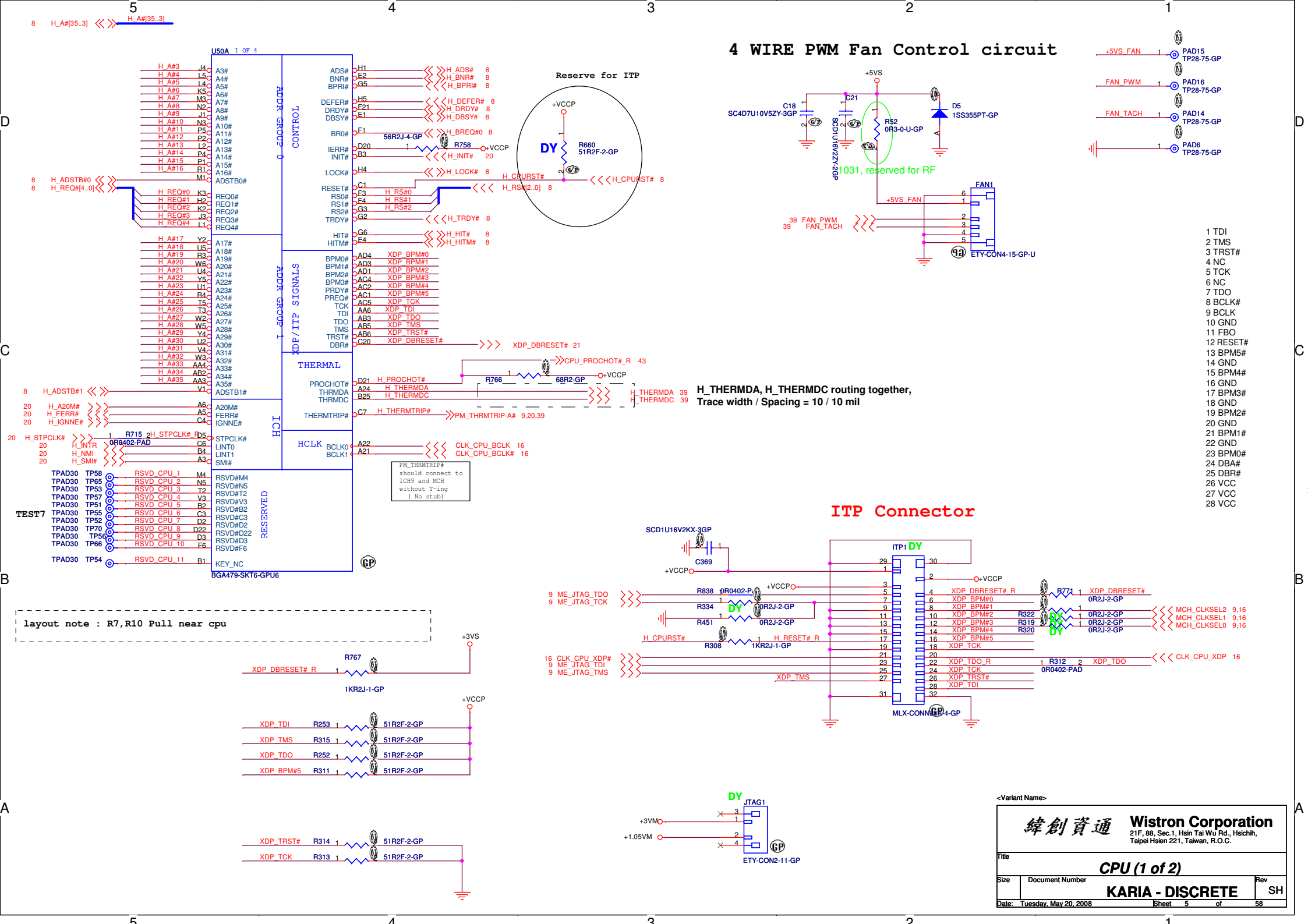
4 WIRE PWM Fan Control circuit
Reserve for ITP
ITP Connector
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil
layout note : R7,R10 Pull near cpu
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
1031, reserved for RF
1 TDI
2 TMS
3 TRST#
4 NC
5 TCK
6 NC
7 TDO
8 BCLK#
9 BCLK
10 GND
11 FBO
12 RESET#
13 BPM5#
14 GND
15 BPM4#
16 GND
17 BPM3#
18 GND
19 BPM2#
20 GND
21 BPM1#
22 GND
23 BPM0#
24 DBA#
25 DBR#
26 VCC
27 VCC
28 VCC
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KARIA - DISCRETE
Tuesday, May 20, 2008

H_DINV#[3..0] H_DINV#[3..0] 8
H_DSTBN#[3..0] H_DSTBN#[3..0] 8
H_DSTBP#[3..0] H_DSTBP#[3..0] 8
H_D#[63..0] H_D#[63..0] 8

U50B 2 OF 4

DATA GRP0 / DATA GRP2

H_D#0	E22	D0#		D32#	Y22	H_D#32	
H_D#1	E24	D1#		D33#	AB24	H_D#33	
H_D#2	E26	D2#		D34#	V24	H_D#34	
H_D#3	G22	D3#		D35#	V26	H_D#35	
H_D#4	F23	D4#		D36#	V23	H_D#36	
H_D#5	G25	D5#		D37#	T22	H_D#37	
H_D#6	E25	D6#		D38#	U25	H_D#38	
H_D#7	E23	D7#		D39#	U23	H_D#39	
H_D#8	K24	D8#		D40#	Y25	H_D#40	
H_D#9	G24	D9#		D41#	W22	H_D#41	
H_D#10	J24	D10#		D42#	Y23	H_D#42	
H_D#11	J23	D11#		D43#	W24	H_D#43	
H_D#12	H22	D12#		D44#	W25	H_D#44	
H_D#13	F26	D13#		D45#	AA23	H_D#45	
H_D#14	K22	D14#		D46#	AA24	H_D#46	
H_D#15	H23	D15#		D47#	AB25	H_D#47	
8 H_DSTBN#0	J26	DSTBN0#		DSTBN2#	Y26	H_DSTBN#2 8	
8 H_DSTBP#0	H26	DSTBP0#		DSTBP2#	AA26	H_DSTBP#2 8	
8 H_DINV#0	H25	DINV0#		DINV2#	U22	H_DINV#2 8	

DATA GRP1 / DATA GRP3

H_D#16	N22	D16#		D48#	AE24	H_D#48	
H_D#17	K25	D17#		D49#	AD24	H_D#49	
H_D#18	P26	D18#		D50#	AA21	H_D#50	
H_D#19	R23	D19#		D51#	AB22	H_D#51	
H_D#20	L23	D20#		D52#	AB21	H_D#52	
H_D#21	M24	D21#		D53#	AC26	H_D#53	
H_D#22	L22	D22#		D54#	AD20	H_D#54	
H_D#23	M23	D23#		D55#	AE22	H_D#55	
H_D#24	P25	D24#		D56#	AE23	H_D#56	
H_D#25	P23	D25#		D57#	AC25	H_D#57	
H_D#26	P22	D26#		D58#	AE21	H_D#58	
H_D#27	T24	D27#		D59#	AD21	H_D#59	
H_D#28	R24	D28#		D60#	AC22	H_D#60	
H_D#29	L25	D29#		D61#	AD23	H_D#61	
H_D#30	T25	D30#		D62#	AE22	H_D#62	
H_D#31	N25	D31#		D63#	AC23	H_D#63	
8 H_DSTBN#1	L26	DSTBN1#		DSTBN3#	AE25	H_DSTBN#3 8	
8 H_DSTBP#1	M26	DSTBP1#		DSTBP3#	AF24	H_DSTBP#3 8	
8 H_DINV#1	N24	DINV1#		DINV3#	AC20	H_DINV#3 8	

CPU_GTLREF0	AD26	GTLREF	MISC	COMP0	R26	COMP0	R765 1 27D4R2F-L1-GP
TEST1	C23	TEST1		COMP1	U26	COMP1	R763 54D9R2F-L1-GP
TEST2	D25	TEST2		COMP2	AA1	COMP2	R254 1 27D4R2F-L1-GP
	C24	TEST3		COMP3	Y1	COMP3	R255 54D9R2F-L1-GP
	AF26	TEST4					
	AF1	TEST5		DPRSTP#	E5	H_DPRSTP# 9,20,43	
	A26	TEST6		DPSLP#	B5	H_DPSLP# 20	
				DPWR#	D24	H_DPWR# 8	
16 CPU_BSEL0	B22	BSEL0		PWRGOOD	D6	H_PWRGD 20	
16 CPU_BSEL1	B23	BSEL1		SLP#	D7	H_CPUSLP# 8	
16 CPU_BSEL2	C21	BSEL2		PSI#	AE6	PSI# 43	

Connect to V Core

BGA479-SKT6-GPU6

Layout notes
Z= 55 Ohm 0.5" MAX for GTLREF

+VCCP
1KR2F-3-GP R303
R304 2KR2F-3-GP
C359 SC1KP50V2KX-1GP
CPU_GTLREF0

R768 R251 1KR2J-1-GP DY DY
R769 DY TEST1 1KR2J-1-GP
R770 DY TEST2 1KR2J-1-GP

Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .

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Please these inside socket cavity on L8(North side Secondary)

Please these inside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(North side Primary)

Please these outside socket cavity on L8(North side Secondary)

Please these outside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(South side Primary)

Please these inside socket cavity on L8(North side Secondary)

layout note: "1D5V_VCCA_S0" as short as possible

Layout Note: Place as close as possible to the CPU VCCA pin.

Connect to V Core

Layout Note: VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note: Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

Close to CPU

NCTF PIN

BGA479-SKT6-GPU6

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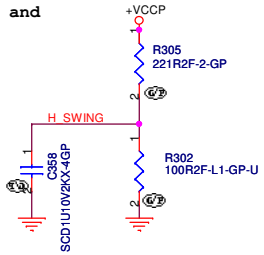
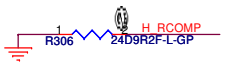
H_SWING routing Trace width and Spacing use 10 / 20 mil

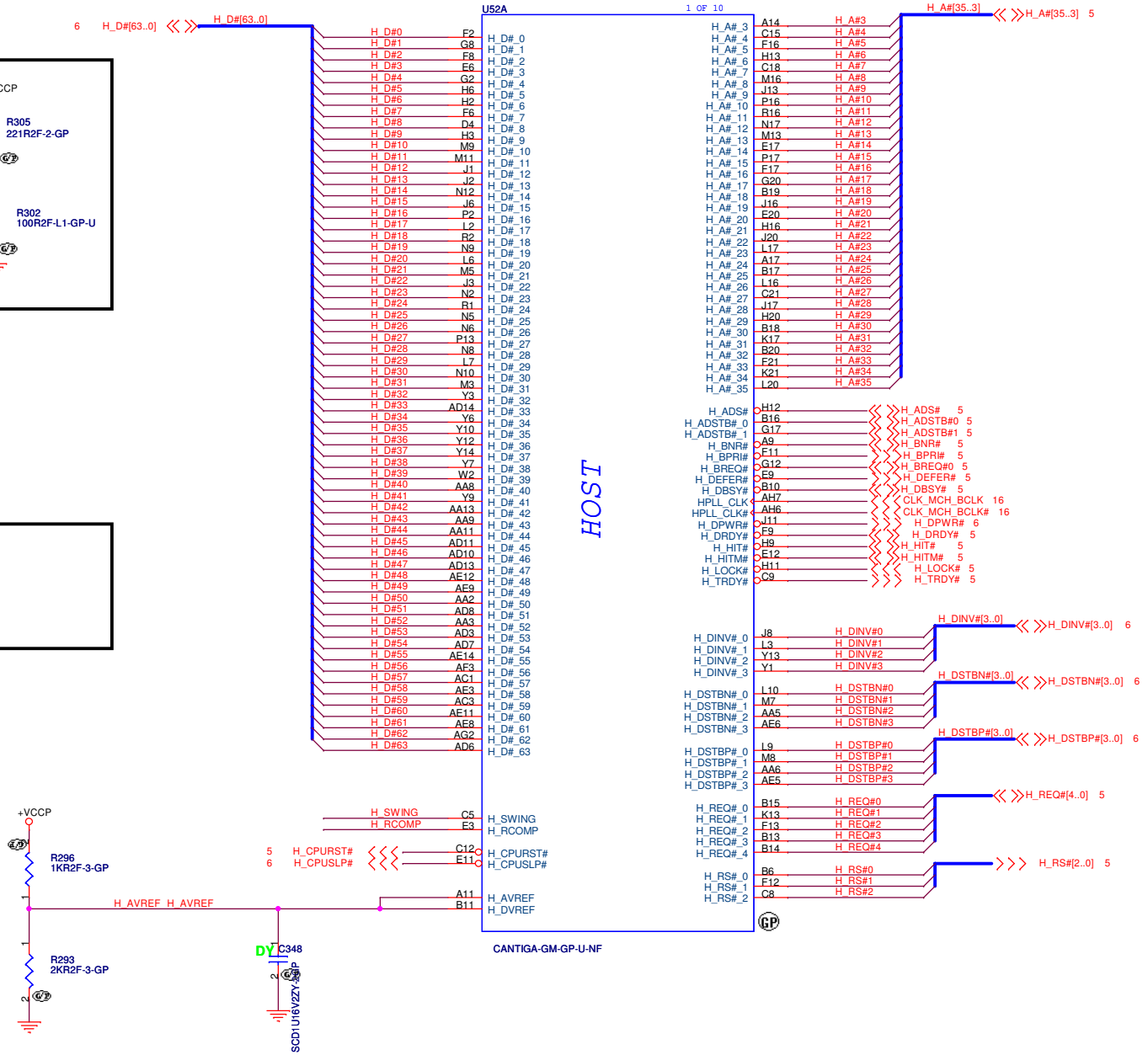
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



<variant_name>

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Title: Cantiga (1 of 6)

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Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1067MHz 011 = FSB 667MHz 010 = FSB 800MHz Others = Reserved
CFG4:3; 8; 11; 14:15; 17; 18	Reserved
CFG5 (DMI select)	Low = DMI x 2 High = DMI x 4 *
CFG6 (ITPM Host Interface)	High = The ITPM Host Interface is disabled * Low = The ITPM Host Interface is enabled
CFG7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher site with no confidentiality High = Intel Management Engine Crypto TLS Cipher suite with confidentiality *
CFG9 (PCIE Graphics Lane)	Low = Reverse Lanes, 15->0, 14->1 etc... High = Normal operation:Lane Numbered in Order *
CFG10 (PCIE Loopback enable)	Low = Enabled High = Disabled *
CFG12 (ALLZ)	Low = ALLZ mode Enabled High = Disabled *
CFG13 (XOR)	Low = XOR mode Enabled High = Disabled *
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled *
CFG19 (DMI Lane Reversal)	Low = Noraml operation: Lane Numbered in Order * High = Reverse Lanes DMI x 4 mode[MCH->ICH]: (0->3, 2->1, 1->2 and 0->3) DMI x 2 mode[MCH->ICH]: (3->0, 2->1)
CFG20 (Digital Display Port (SDVO/DP /iHDMI) Concurrent with PCIE)	Low = Only Digital Display Port (SDVO/iHDMI) or PCIE is operational * High = Digital Display Port (SDVO/DP/iHDMI) and PCIE are operating simulatneously via the PEG port
SDVO_CTRLDATA (SDVO Present)	Low = No SDVO Card Present * High = SDVO Card Present
L_DDC_DATA (Local Flat Panel (LFP) Present)	Low = LFP Disabled * High = LFP Card Present; PCIE disabled
DDPC_CTRLDATA (Digital Display Present)	Low = DisplayPort Disabled * High = DisplayPort Device Present

Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.
49.9 OHM PN:64.49R95.6DL

FSB setting

CFG 5, 7, 9, 10, 12, 13, 16, 19, 20
Teenah = 4.02K
Cantiga = 2.2K

Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time

CANTIGA-GM-GP-U-NF

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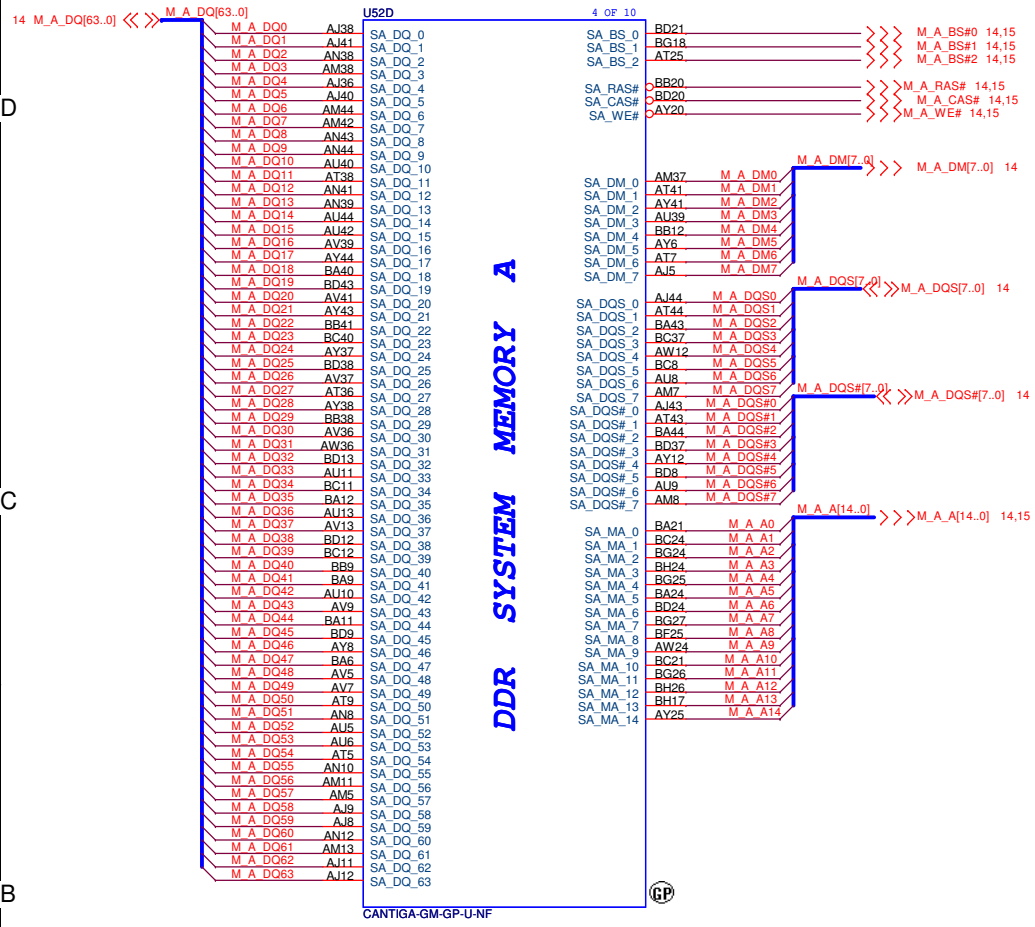

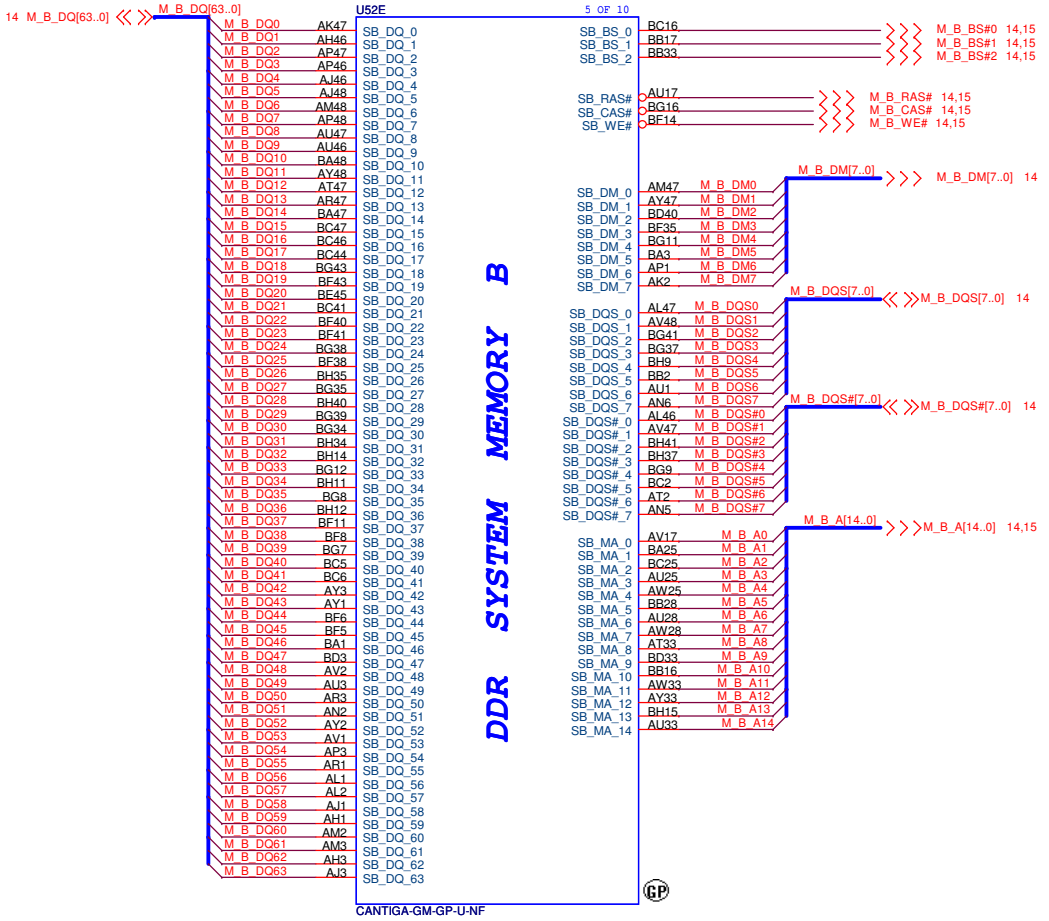

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Title: *Cantiga (3 of 6)*

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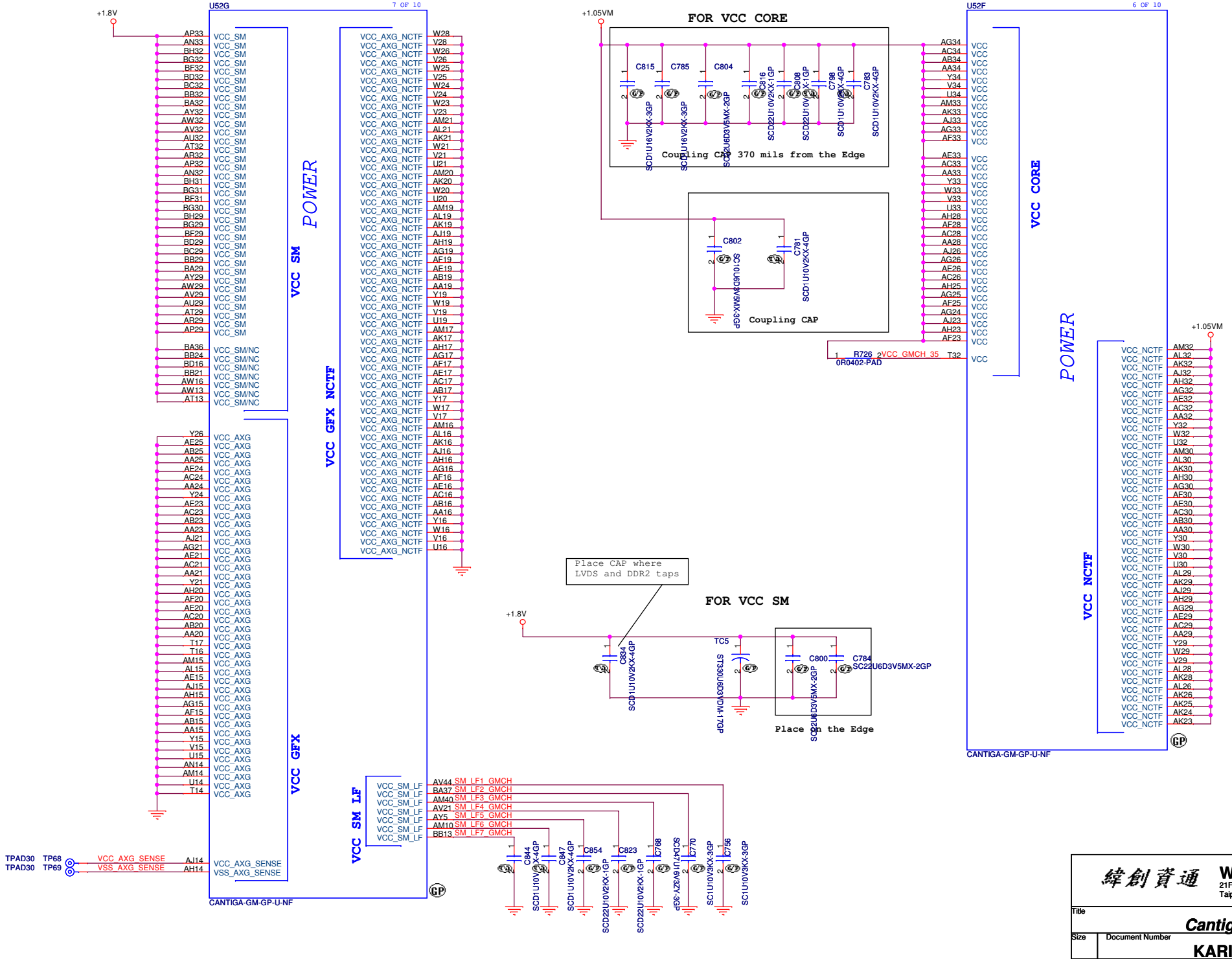

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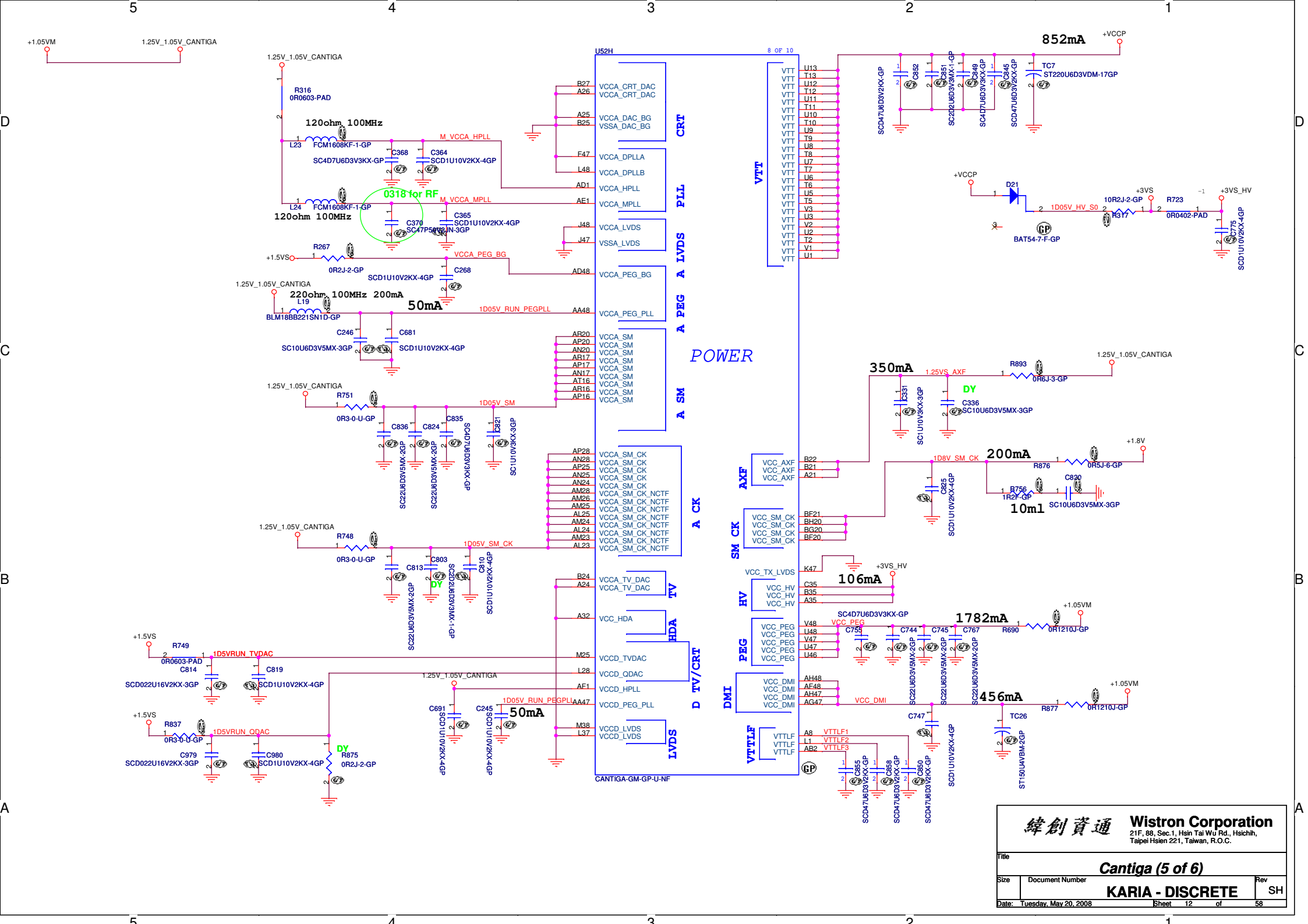
POWER
U52H
CANTIGA-GM-GP-U-NF
8 OF 10
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
852mA
350mA
200mA
106mA
1782mA
456mA
50mA
220ohm 100MHz 200mA
120ohm 100MHz
0318 for RF
10ml
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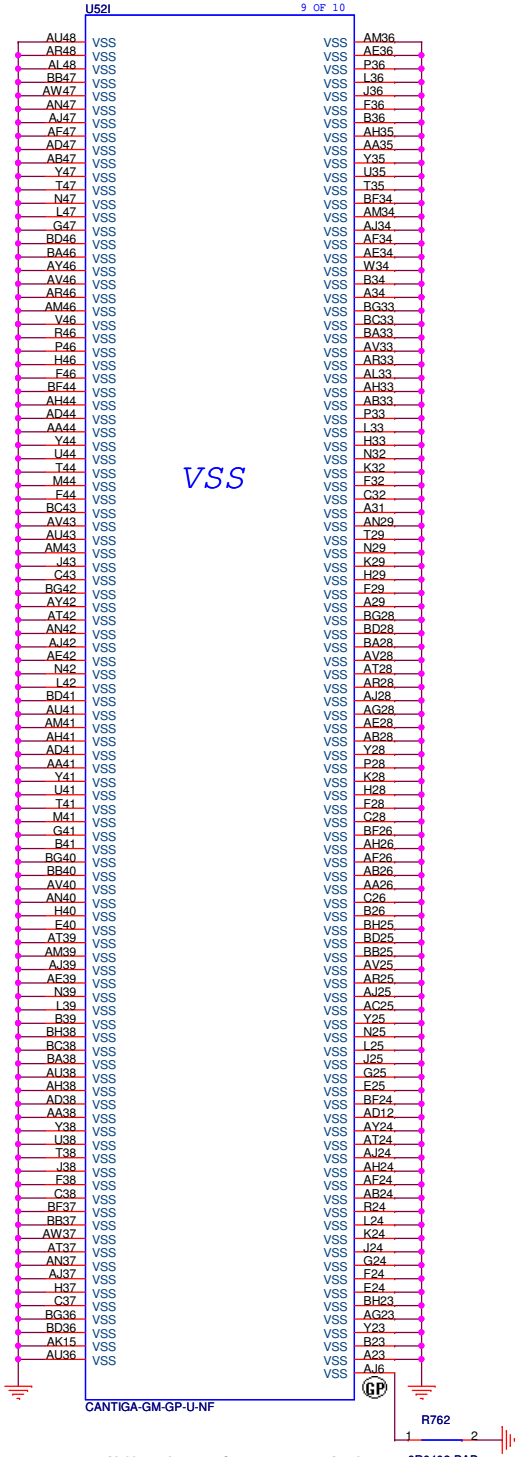
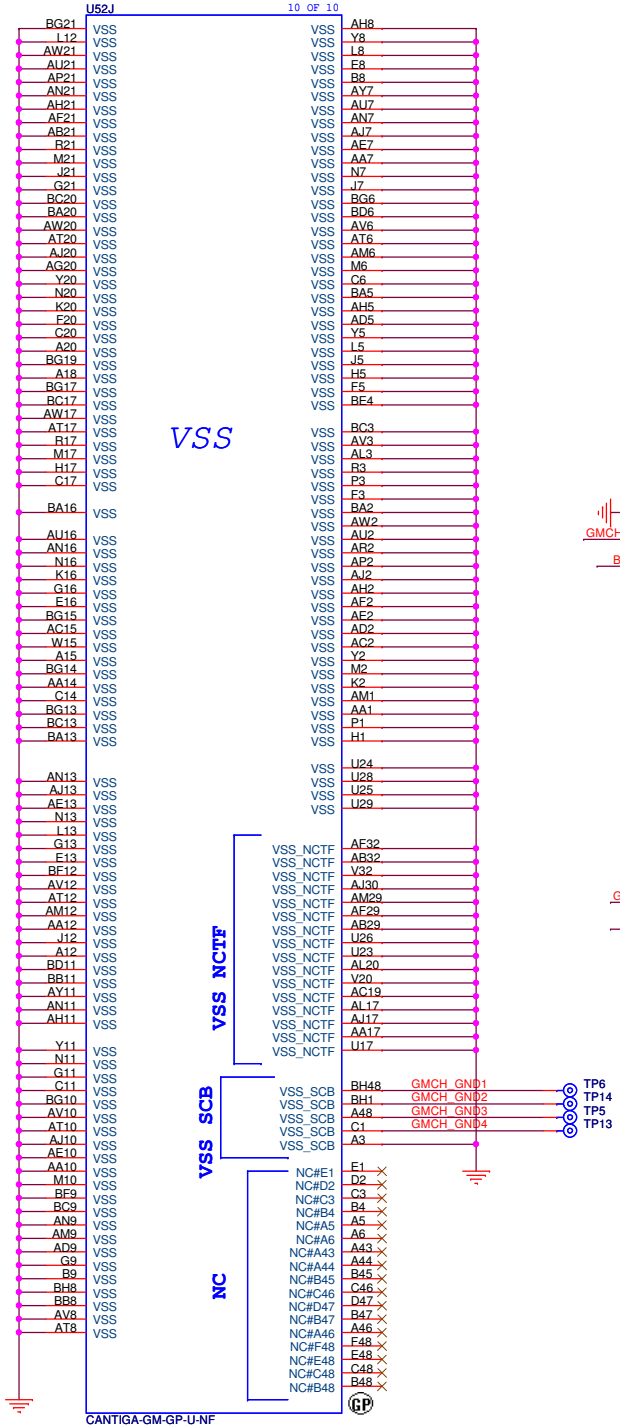
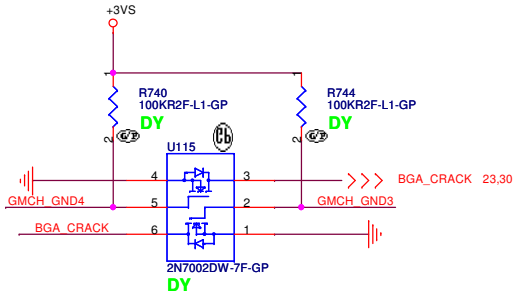
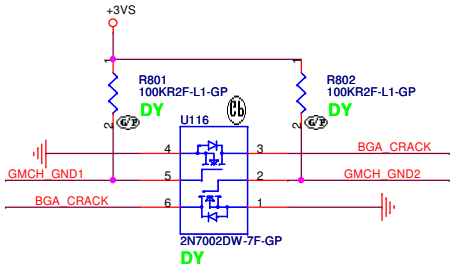
Cantiga (5 of 6)
KARIA - DISCRETE
Tuesday, May 20, 2008









NCTF PIN

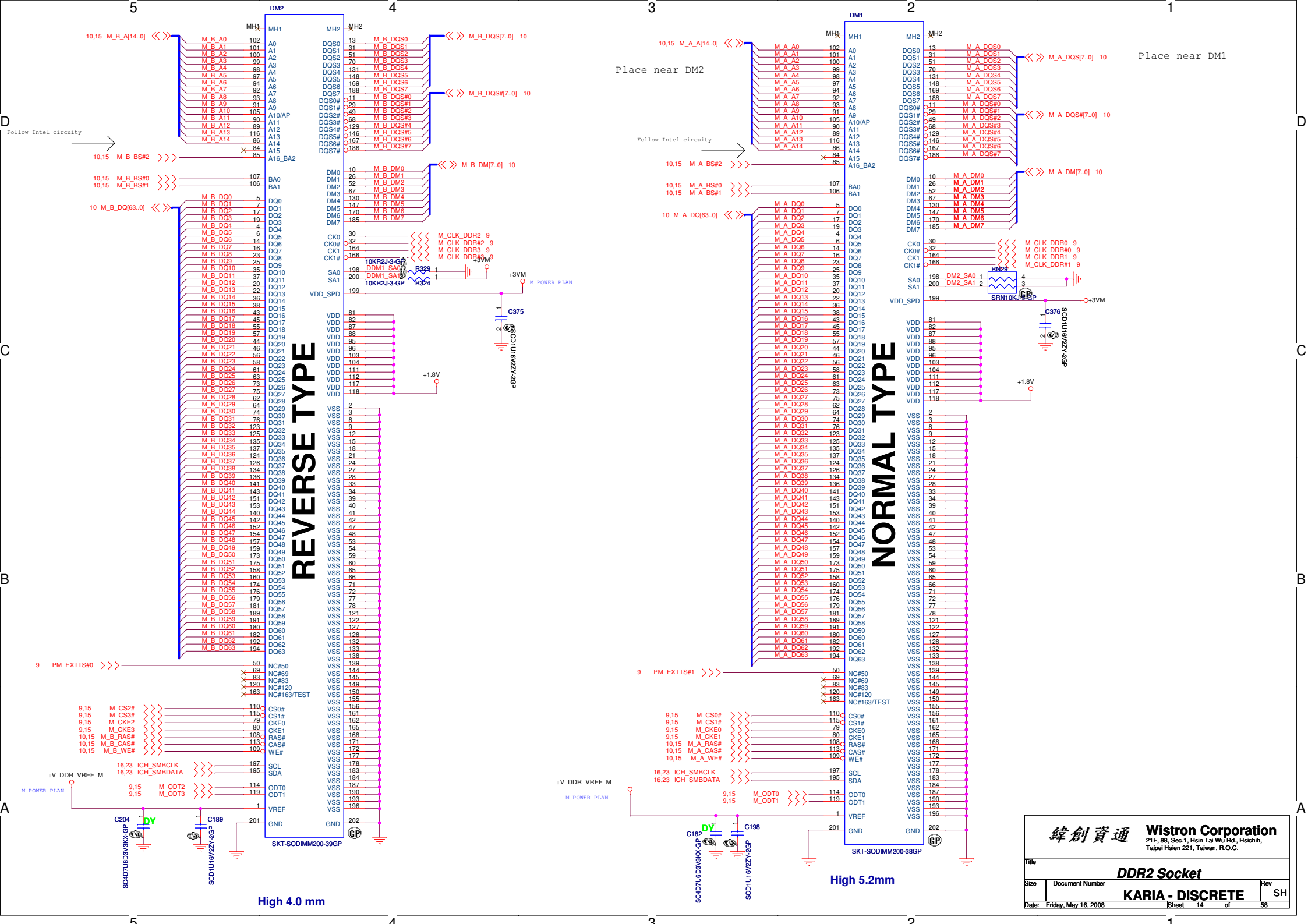
TP6
TP14
TP5
TP13

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cantiga (6 of 6)***

Size | Document Number: **KARIA - DISCRETE** | Rev: SH

Date: Monday, May 19, 2008 | Sheet 13 of 58


DM2
REVERSE TYPE
SKT-SODIMM200-39GP
Follow Intel circuitry
Place near DM2
M POWER PLAN
+3VM
+1.8V
+V_DDR_VREF_M
C204
C189
SC4D7U6D3V3KX-GP
SCD1U16V2ZY-2GP
10KR2J-3-GP
R329
R324
C375
High 4.0 mm
DM1
NORMAL TYPE
SKT-SODIMM200-38GP
Place near DM1
RN29
SRN10KJ-3-GP
C376
C182
C198
High 5.2mm
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 Socket
Size
Document Number
KARIA - DISCRETE
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PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

+0.9V

RN18 SRN56J-5-GP
- M_A_A14
- M_A_A11
- M_A_A7
- M_CKE1 9,14

RN44 SRN56J-5-GP
- M_B_BS#1 10,14
- M_B_RAS# 10,14
- M_CS2# 9,14
- M_ODT2 9,14

RN26 SRN56J-5-GP
- M_B_A13
- M_ODT1 9,14
- M_CS1# 9,14

RN43 SRN56J-5-GP
- M_B_A6
- M_B_A4
- M_B_A2
- M_B_A0

RN21 SRN56J-5-GP
- M_A_A1
- M_A_A3
- M_A_A5
- M_A_A8

RN24 SRN56J-5-GP
- M_A_CAS# 10,14
- M_A_WE# 10,14
- M_A_BS#0 10,14
- M_A_A10

RN23 SRN56J-5-GP
- M_B_A8
- M_A_BS#1 10,14
- M_A_RAS# 10,14
- M_CS0# 9,14

RN42 SRN56J-5-GP
- M_B_A14
- M_B_A11
- M_B_A7
- M_CKE3 9,14

RN25 SRN56J-5-GP
- M_A_A13
- M_B_A5
- M_B_A3
- M_ODT0 9,14

RN19 SRN56J-5-GP
- M_A_A9
- M_A_A12
- M_A_BS#2 10,14
- M_CKE0 9,14

RN28 SRN56J-5-GP
- M_B_CAS# 10,14
- M_CS3# 9,14
- M_ODT3 9,14

RN27 SRN56J-5-GP
- M_B_A1
- M_B_A10
- M_B_BS#0 10,14
- M_B_WE# 10,14

RN20 SRN56J-5-GP
- M_CKE2 9,14
- M_B_BS#2 10,14
- M_B_A12
- M_A_A6

RN22 SRN56J-5-GP
- M_A_A4
- M_A_A2
- M_A_A0
- M_B_A9

M_A_A[14..0] <<>> M_A_A[14..0] 10,14

M_B_A[14..0] <<>> M_B_A[14..0] 10,14

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

+0.9V

C322 C356 C284 C343 C346 C838 C806 C774 C316 C279 C760 C252 C753 C294 — SCD1U16V2ZY-2GP

C772 C287 C350 C275 C286 C347 C253 C282 C251 C285 C832 C309 C277 — SCD1U16V2ZY-2GP

Place these Caps near DM1

+1.8V

C811 C330 C361 C818 C786 — SC2D2U6D3V3MX-1-GP

TC17 SE330U2D5VDM-LGP

C812 C843 C833 C805 — SCD1U16V2ZY-2GP

Place the Cap near MCH

+1.8V

TC1 SE330U2D5VDM-LGP

Place these Caps near DM2

+1.8V

C311 C328 C334 C344 C297 — SC2D2U6D3V3MX-1-GP

TC23 SE330U2D5VDM-LGP

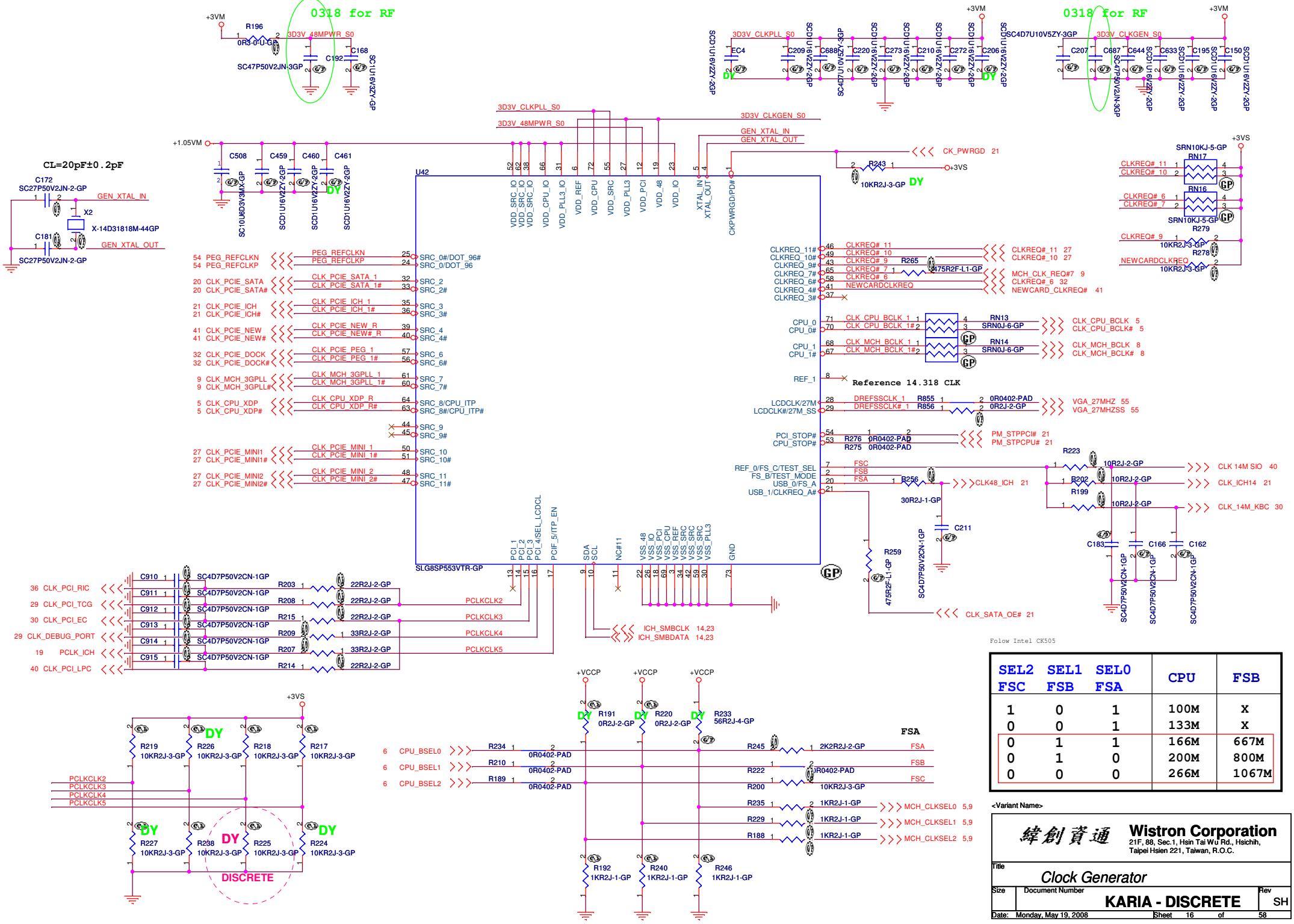
C771 C315 C314 C822 — SCD1U16V2ZY-2GP

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Termination Resistor***

Size | Document Number: **KARIA - DISCRETE** | Rev: SH

Date: Friday, May 16, 2008 | Sheet 15 of 58


0318 for RF
0318 for RF
CL=20pF±0.2pF
U42
SLG8SP553VTR-GP
Reference 14.318 CLK
Folow Intel CK505
DISCRETE
SEL2 FSC | SEL1 FSB | SEL0 FSA | CPU | FSB
1 | 0 | 1 | 100M | X
0 | 0 | 1 | 133M | X
0 | 1 | 1 | 166M | 667M
0 | 1 | 0 | 200M | 800M
0 | 0 | 0 | 266M | 1067M
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator
Size
Document Number
KARIA - DISCRETE
Rev
SH
Date: Monday, May 19, 2008
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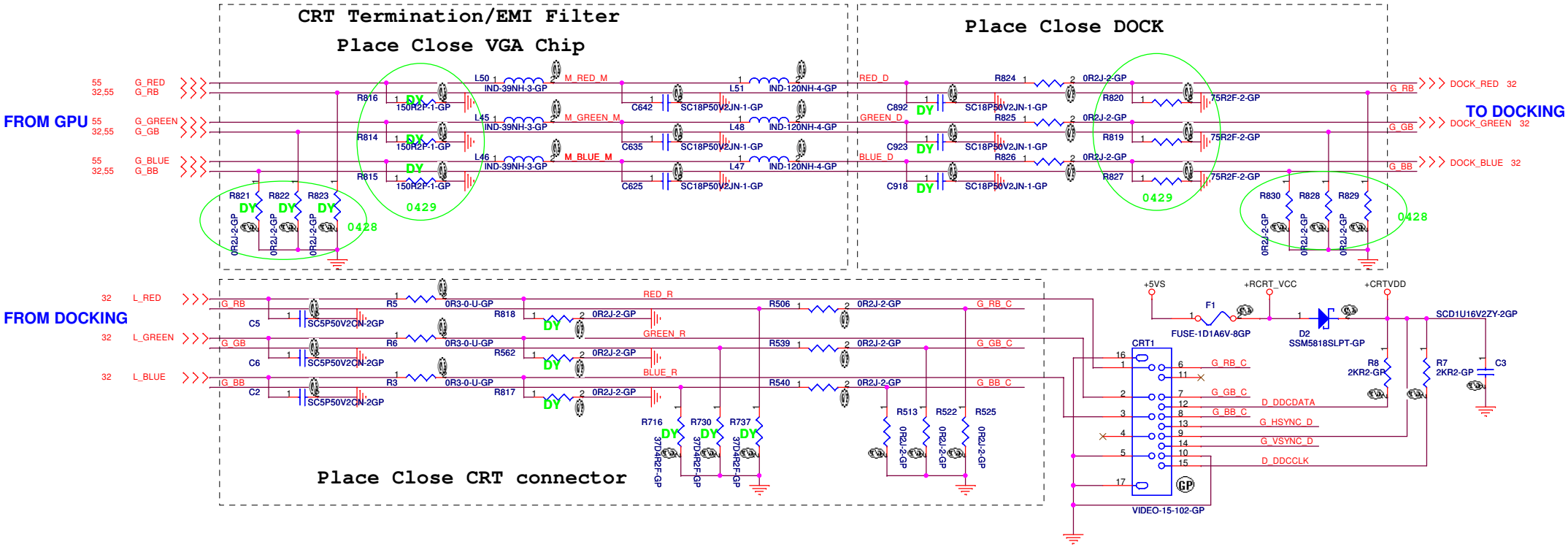
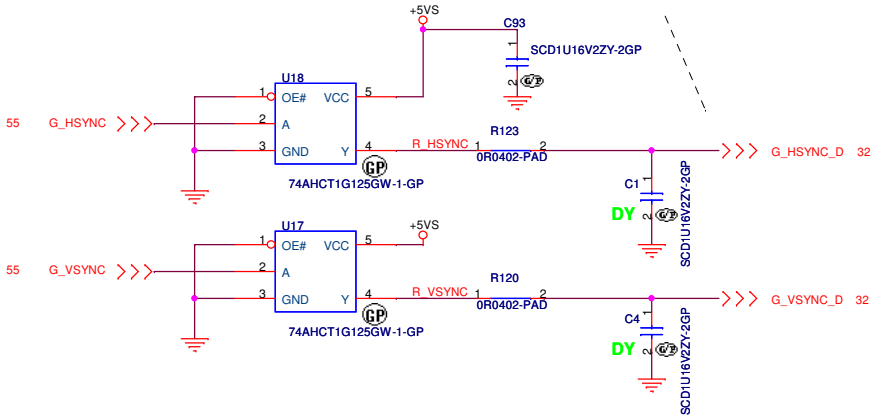
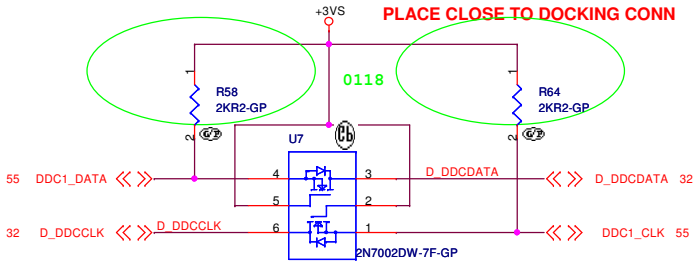
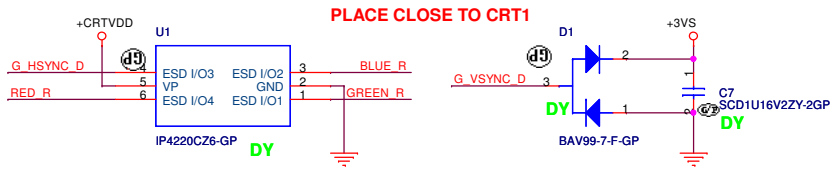
CRT



Layout Note : HSYNC & VSYNC SHOULD BE ROUTED TO DOCK CRT CONN. ,THEN TO SYSTEM CRT CONN.

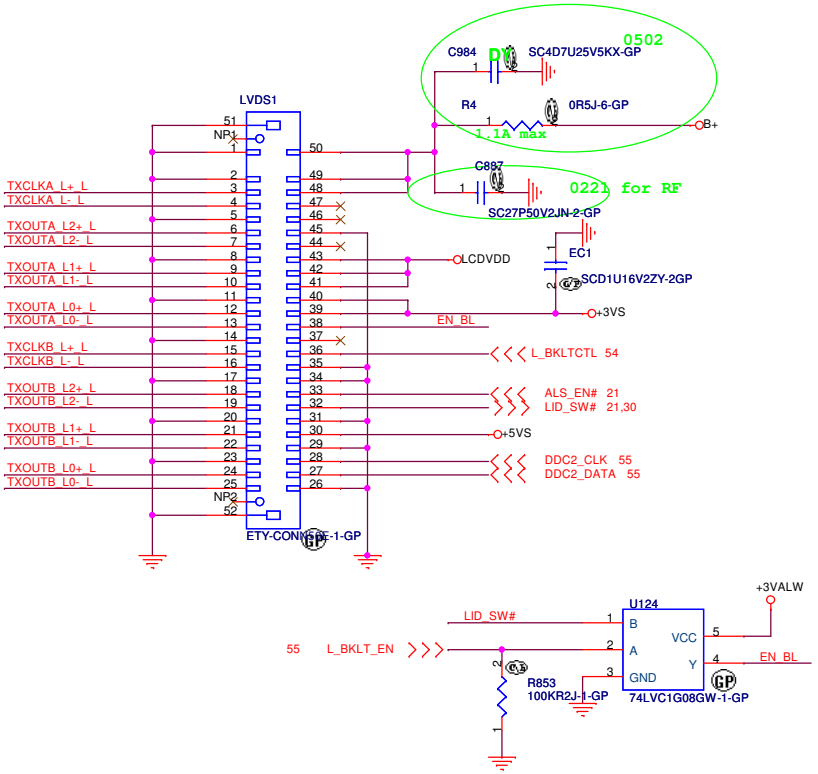




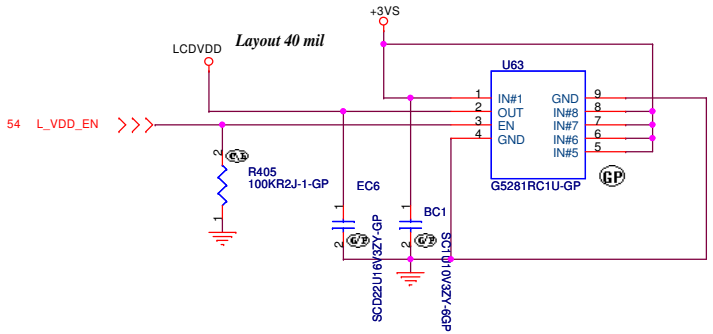


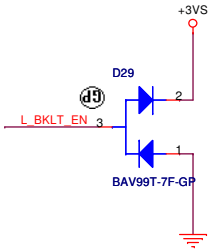
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT CONNECTOR***	
Size A3	Document Number **KARIA - DISCRETE**	Rev SH
Date: Monday, May 19, 2008	Sheet 17 of 58	

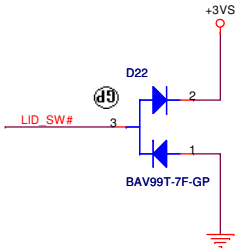
LVDS CONN

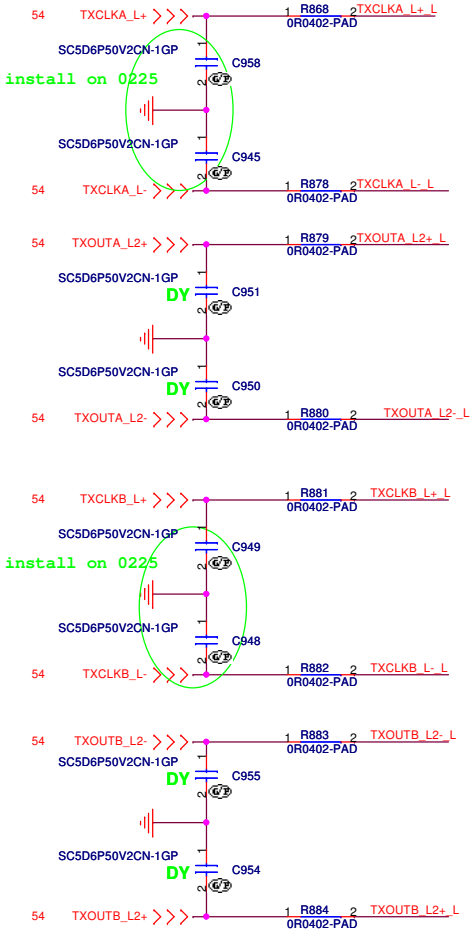


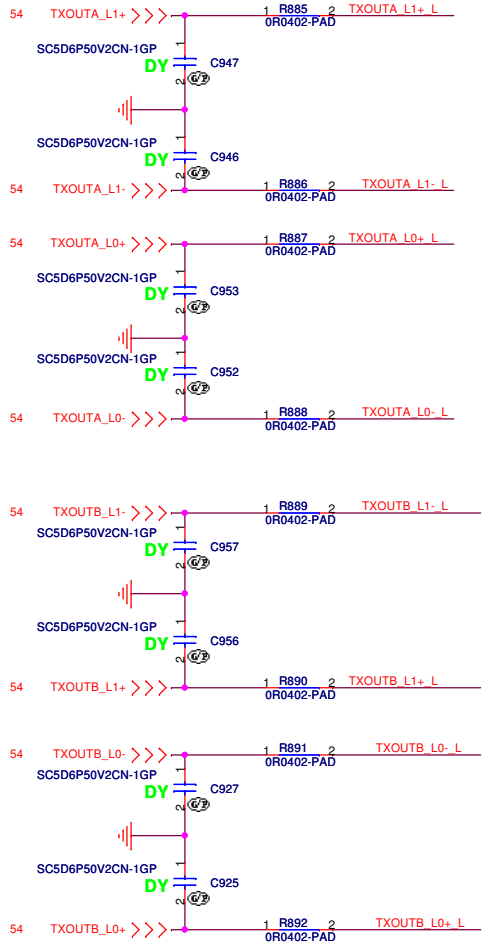
LCD POWER CIRCUIT









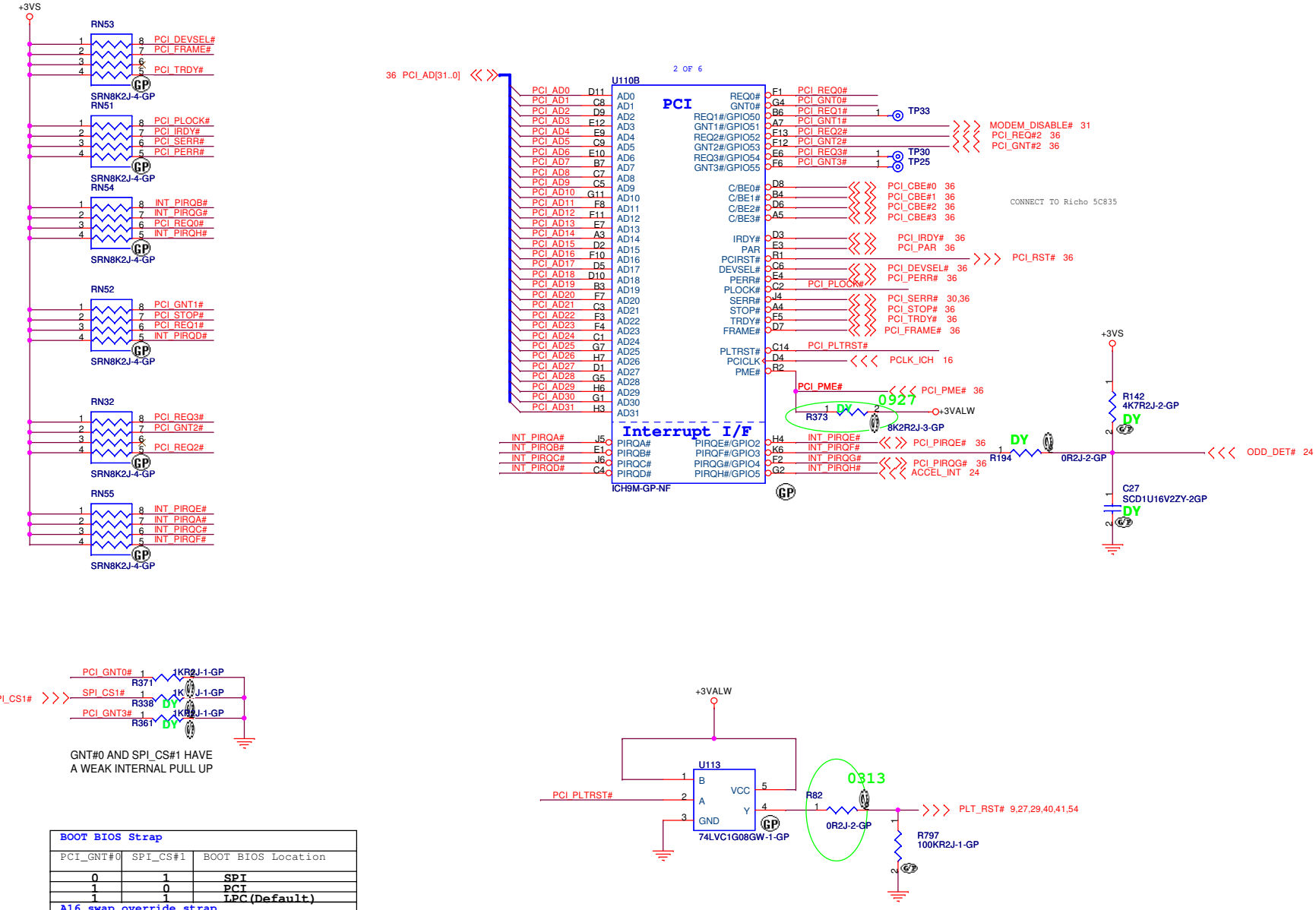


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN.

Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

Date: Friday, May 16, 2008 | Sheet 18 of 58



BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (1 of 5)

Size | Document Number: KARIA - DISCRETE | Rev: SH

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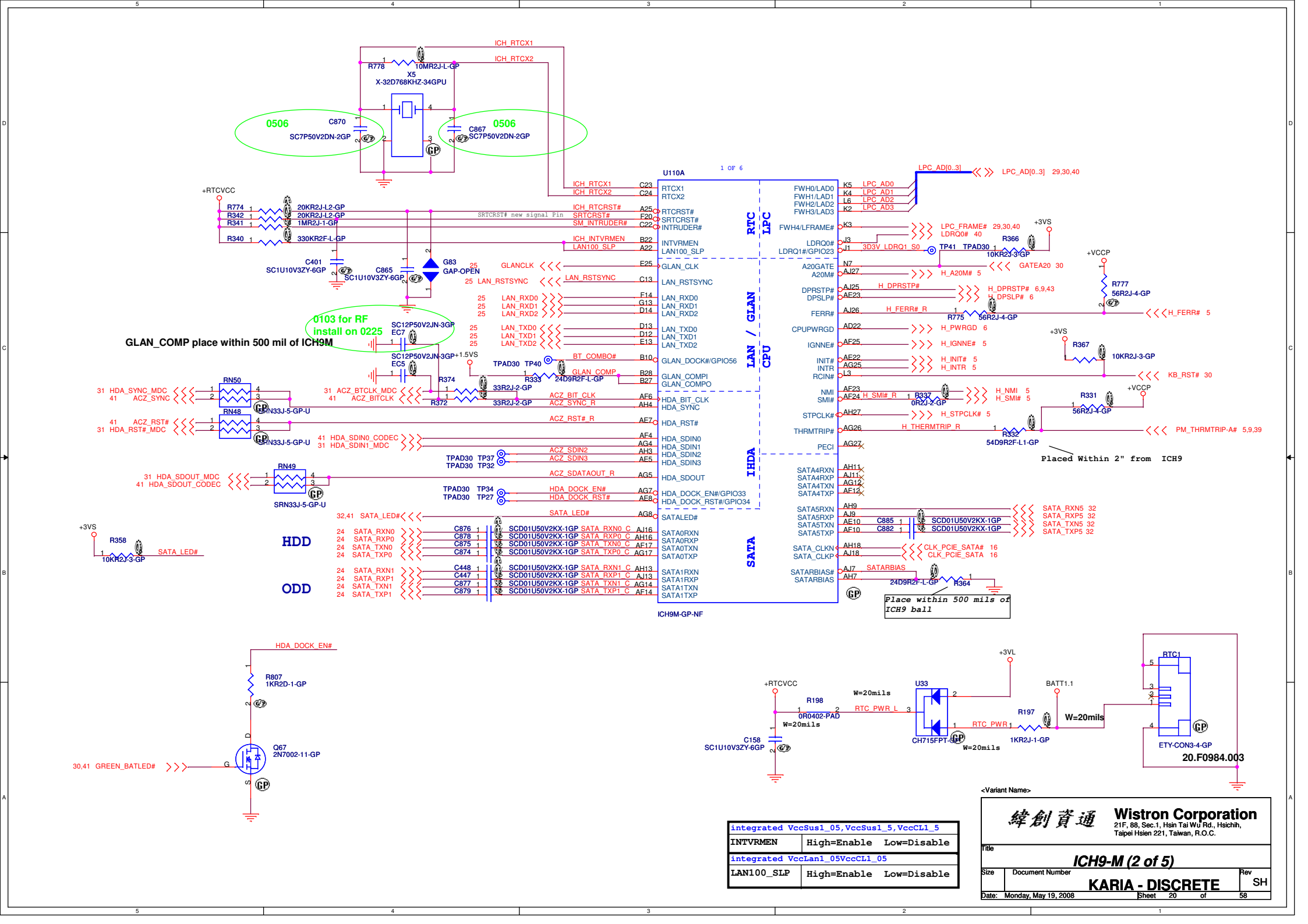
ICH_RTCX1
ICH_RTCX2
R778 10MR2J-L-GP
X5
X-32D768KHZ-34GPU
0506
C870 SC7P50V2DN-2GP
C867 SC7P50V2DN-2GP
0506
U110A
1 OF 6
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
ICH9M-GP-NF
+RTCVCC
R774 20KR2J-L2-GP
R342 20KR2J-L2-GP
R341 1MR2J-1-GP
R340 330KR2F-L-GP
C401 SC1U10V3ZY-6GP
C865 SC1U10V3ZY-6GP
G83 GAP-OPEN
SRTCRST# new signal Pin
ICH_RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
LAN100_SLP
GLANCLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
0103 for RF
install on 0225
SC12P50V2JN-3GP EC7
GLAN_COMP place within 500 mil of ICH9M
SC12P50V2JN-3GP EC5
+1.5VS
TPAD30 TP40
BT_COMBO#
GLAN_COMP
R333 24D9R2F-L-GP
R374
R372
33R2J-2-GP
33R2J-2-GP
RN50
RN48
RN49
SRN33J-5-GP-U
31 HDA_SYNC_MDC
41 ACZ_SYNC
31 ACZ_BTCLK_MDC
41 ACZ_BITCLK
41 ACZ_RST#
31 HDA_RST#_MDC
31 HDA_SDOUT_MDC
41 HDA_SDOUT_CODEC
41 HDA_SDIN0_CODEC
31 HDA_SDIN1_MDC
ACZ_BIT_CLK
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDIN2
ACZ_SDIN3
ACZ_SDATAOUT_R
HDA_DOCK_EN#
HDA_DOCK_RST#
SATA_LED#
TPAD30 TP37
TPAD30 TP32
TPAD30 TP34
TPAD30 TP27
+3VS
R358 10KR2J-3-GP
SATA_LED#
HDD
ODD
C876 SCD01U50V2KX-1GP SATA_RXN0_C
C878 SCD01U50V2KX-1GP SATA_RXP0_C
C875 SCD01U50V2KX-1GP SATA_TXN0_C
C874 SCD01U50V2KX-1GP SATA_TXP0_C
C448 SCD01U50V2KX-1GP SATA_RXN1_C
C447 SCD01U50V2KX-1GP SATA_RXP1_C
C877 SCD01U50V2KX-1GP SATA_TXN1_C
C879 SCD01U50V2KX-1GP SATA_TXP1_C
24 SATA_RXN0
24 SATA_RXP0
24 SATA_TXN0
24 SATA_TXP0
24 SATA_RXN1
24 SATA_RXP1
24 SATA_TXN1
24 SATA_TXP1
LPC_AD[0..3]
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME# 29,30,40
LDRQ0# 40
3D3V_LDRQ1_S0
TP41 TPAD30
R366 10KR2J-3-GP
+3VS
A20GATE
A20M#
H_A20M# 5
GATEA20 30
DPRSTP#
DPSLP#
H_DPRSTP# 6,9,43
H_DPSLP# 6
FERR#
H_FERR# R
R775 56R2J-4-GP
R777 56R2J-4-GP
+VCCP
H_FERR# 5
CPUPWRGD
H_PWRGD 6
IGNNE#
H_IGNNE# 5
INIT#
INTR
RCIN#
H_INIT# 5
H_INTR 5
R367 10KR2J-3-GP
+3VS
KB_RST# 30
NMI
SMI#
H_SMI# R
R337 0R2J-2-GP
H_NMI 5
H_SMI# 5
R331 56R2J-4-GP
+VCCP
STPCLK#
H_STPCLK# 5
THRMTRIP#
H_THERMTRIP_R
R332 54D9R2F-L1-GP
PM_THRMTRIP-A# 5,9,39
Placed Within 2" from ICH9
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
C885 SCD01U50V2KX-1GP
C882 SCD01U50V2KX-1GP
SATA_RXN5 32
SATA_RXP5 32
SATA_TXN5 32
SATA_TXP5 32
SATA_CLKN
SATA_CLKP
CLK_PCIE_SATA# 16
CLK_PCIE_SATA 16
SATARBIAS#
SATARBIAS
R364 24D9R2F-L-GP
Place within 500 mils of ICH9 ball
HDA_DOCK_EN#
R807 1KR2D-1-GP
Q67 2N7002-11-GP
30,41 GREEN_BATLED#
+RTCVCC
R198 0R0402-PAD
W=20mils
RTC_PWR_L
U33 CH715FPT-GP
+3VL
BATT1.1
R197 1KR2J-1-GP
RTC_PWR
C158 SC1U10V3ZY-6GP
RTC1 ETY-CON3-4-GP
20.F0984.003
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 5)
Size
Document Number
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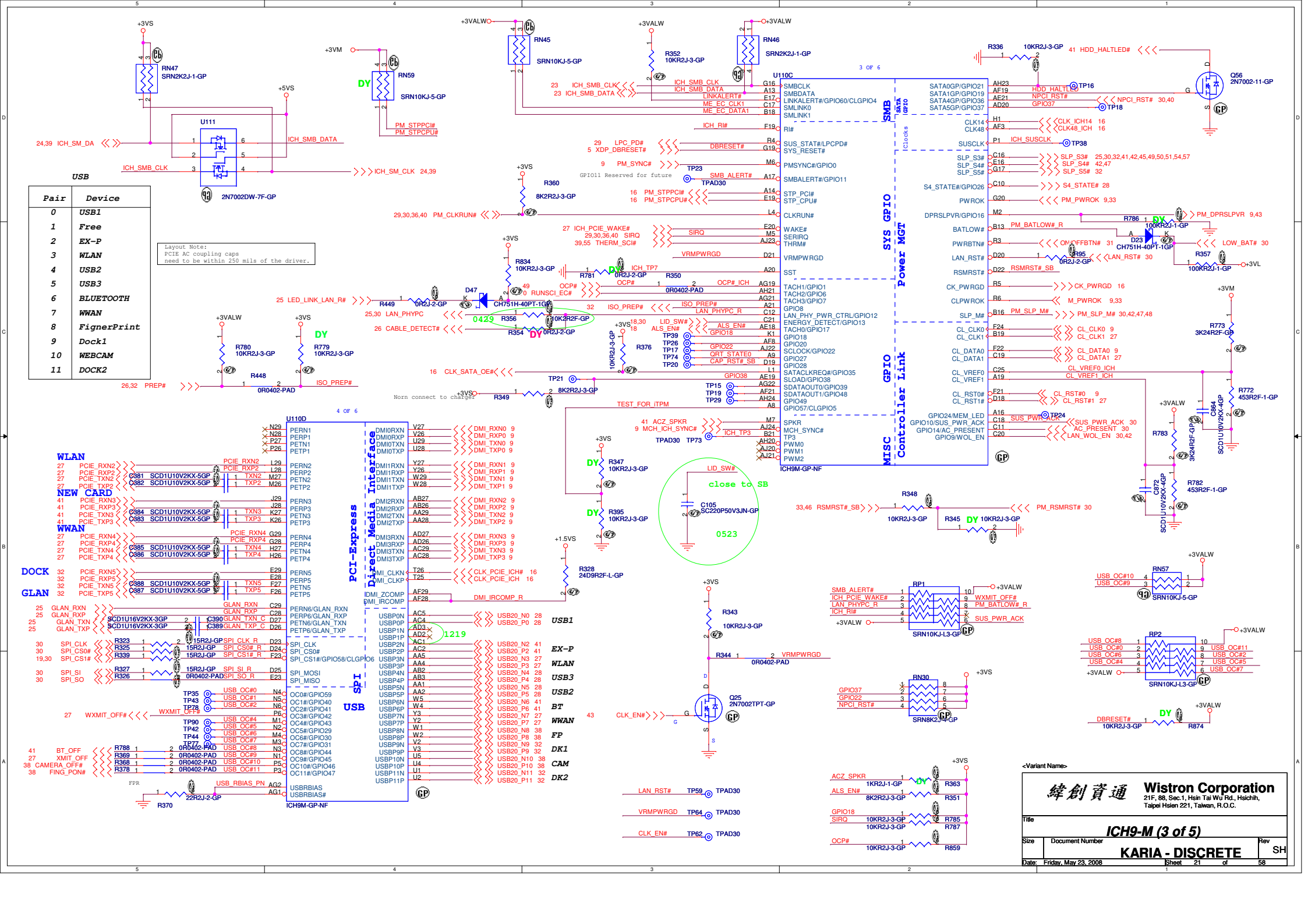
USB
Pair | Device
0 | USB1
1 | Free
2 | EX-P
3 | WLAN
4 | USB2
5 | USB3
6 | BLUETOOTH
7 | WWAN
8 | FignerPrint
9 | Dock1
10 | WEBCAM
11 | DOCK2
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
U110C
ICH9M-GP-NF
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
MISC
Controller Link
U110D
ICH9M-GP-NF
PCI-Express
Direct Media Interface
SPI
USB
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6/GLAN_RXN
PERP6/GLAN_RXP
PETN6/GLAN_TXN
PETP6/GLAN_TXP
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
IDMI_ZCOMP
IDMI_IRCOMP
SPI_CLK
SPI_CS0#
SPI_CS1#/GPIO58/CLGPIO6
SPI_MOSI
SPI_MISO
OC0#/GPIO59
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO29
OC6#/GPIO30
OC7#/GPIO31
OC8#/GPIO44
OC9#/GPIO45
OC10#/GPIO46
OC11#/GPIO47
USBRBIAS
USBRBIAS#
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
WLAN
NEW CARD
WWAN
DOCK
GLAN
USB1
EX-P
WLAN
USB3
USB2
BT
WWAN
FP
DK1
CAM
DK2
1219
close to SB
C105
SC220P50V3JN-GP
0523
Norn connect to charger
TEST_FOR_iTPM
Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (3 of 5)
Size
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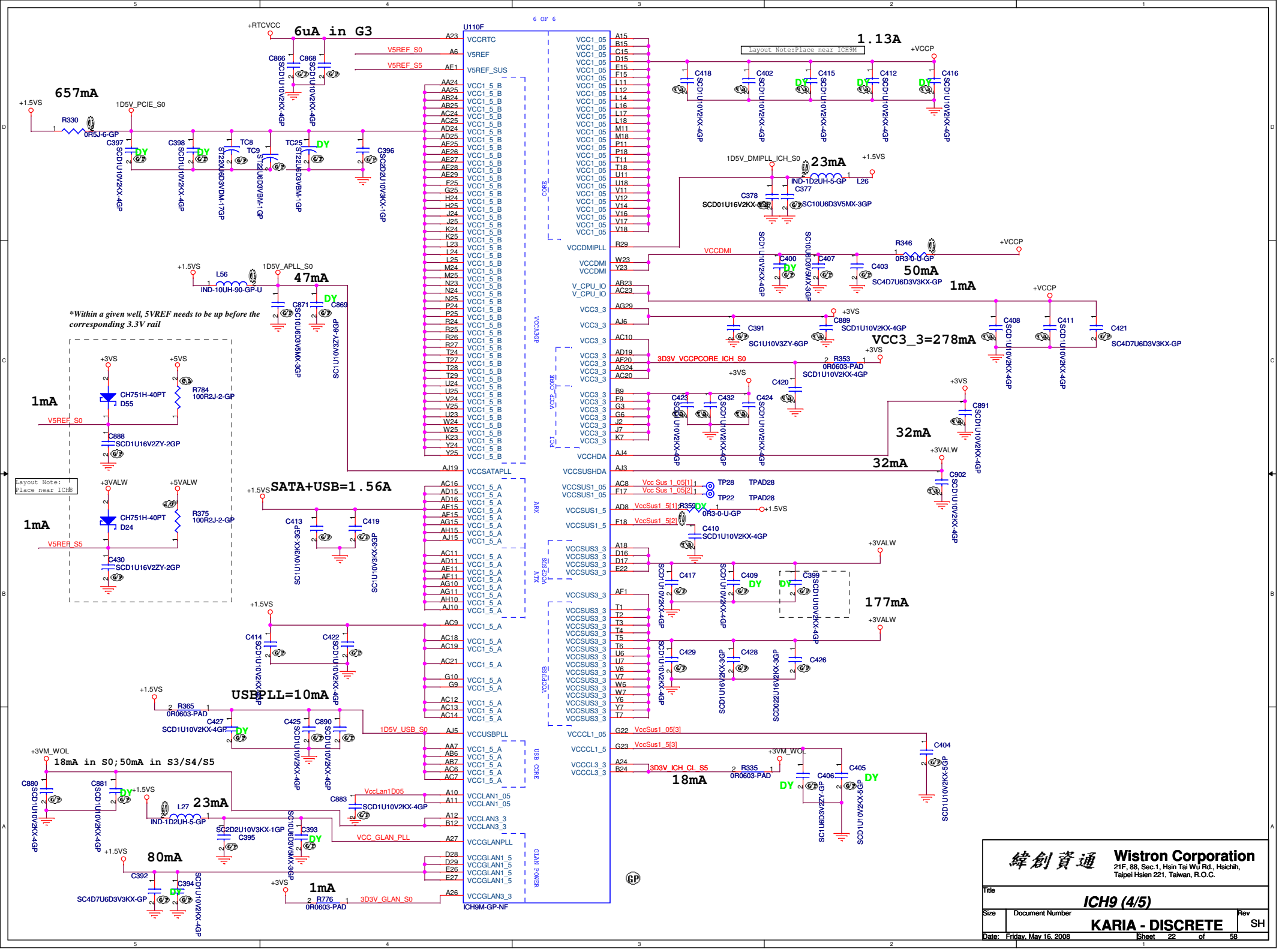
6 OF 6
U110F
ICH9M-GP-NF
6uA in G3
657mA
1.13A
23mA
47mA
50mA
1mA
VCC3_3=278mA
32mA
32mA
177mA
SATA+USB=1.56A
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
23mA
80mA
1mA
1mA
18mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
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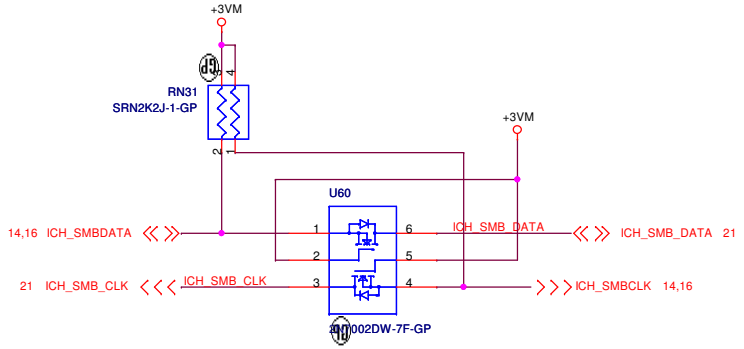
U110E

AA26	VSS	VSS	H5
AA27	VSS	VSS	J23
AA3	VSS	VSS	J26
AA6	VSS	VSS	J27
AB1	VSS	VSS	AC22
AA23	VSS	VSS	K28
AB28	VSS	VSS	K29
AB29	VSS	VSS	L13
AB4	VSS	VSS	L15
AB5	VSS	VSS	L2
AC17	VSS	VSS	L26
AC26	VSS	VSS	L27
AC27	VSS	VSS	L5
AC3	VSS	VSS	L7
AD1	VSS	VSS	M12
AD10	VSS	VSS	M13
AD12	VSS	VSS	M14
AD13	VSS	VSS	M15
AD14	VSS	VSS	M16
AD17	VSS	VSS	M17
AD18	VSS	VSS	M23
AD21	VSS	VSS	M28
AD28	VSS	VSS	M29
AD29	VSS	VSS	N11
AD4	VSS	VSS	N12
AD5	VSS	VSS	N13
AD6	VSS	VSS	N14
AD7	VSS	VSS	N15
AD9	VSS	VSS	N16
AE12	VSS	VSS	N17
AE13	VSS	VSS	N18
AE14	VSS	VSS	N26
AE16	VSS	VSS	N27
AE17	VSS	VSS	P12
AE2	VSS	VSS	P13
AE20	VSS	VSS	P14
AE24	VSS	VSS	P15
AE3	VSS	VSS	P16
AE4	VSS	VSS	P17
AE6	VSS	VSS	P2
AE9	VSS	VSS	P23
AF13	VSS	VSS	P28
AF16	VSS	VSS	P29
AF18	VSS	VSS	P4
AF22	VSS	VSS	P7
AH26	VSS	VSS	R11
AF26	VSS	VSS	R12
AF27	VSS	VSS	R13
AF5	VSS	VSS	R14
AF7	VSS	VSS	R15
AF9	VSS	VSS	R16
AG13	VSS	VSS	R17
AG16	VSS	VSS	R18
AG18	VSS	VSS	R28
AG20	VSS	VSS	T12
AG23	VSS	VSS	T13
AG3	VSS	VSS	T14
AG6	VSS	VSS	T15
AG9	VSS	VSS	T16
AH12	VSS	VSS	T17
AH14	VSS	VSS	T23
AH17	VSS	VSS	B26
AH19	VSS	VSS	U12
AH2	VSS	VSS	U13
AH22	VSS	VSS	U14
AH25	VSS	VSS	U15
AH28	VSS	VSS	U16
AH5	VSS	VSS	U17
AH8	VSS	VSS	AD23
AJ12	VSS	VSS	U26
AJ14	VSS	VSS	U27
AJ17	VSS	VSS	U3
AJ8	VSS	VSS	V1
B11	VSS	VSS	V13
B14	VSS	VSS	V15
B17	VSS	VSS	V23
B2	VSS	VSS	V28
B20	VSS	VSS	V29
B23	VSS	VSS	V4
B5	VSS	VSS	V5
B8	VSS	VSS	W26
C26	VSS	VSS	W27
C27	VSS	VSS	W3
E11	VSS	VSS	Y1
E14	VSS	VSS	Y28
E18	VSS	VSS	Y29
E2	VSS	VSS	Y4
E21	VSS	VSS	Y5
E24	VSS	VSS	AG28
E5	VSS	VSS	AH6
E8	VSS	VSS	AF2
F16	VSS	VSS	B25
F28	VSS		
F29	VSS	A1	ICH_GND1 → TP76
G12	VSS	A2	
G14	VSS	A28	
G18	VSS	A29	ICH_GND2 → TP71
G21	VSS	AH1	
G24	VSS	AH29	
G26	VSS	AJ1	ICH_GND3 → TP75
G27	VSS	AJ2	
G8	VSS	AJ28	
H2	VSS	AJ29	ICH_GND4 → TP72
H23	VSS	B1	
H28	VSS	B29	
H29	VSS		

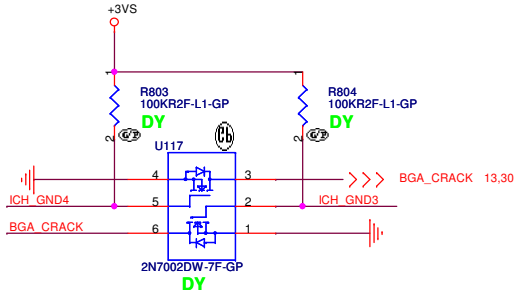
ICH9M-GP-NF

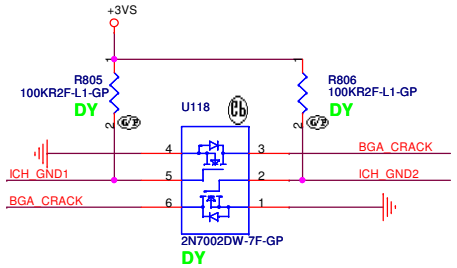
NCTF PIN



Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS





緯創資通 **Wistron Corporation**
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Title: ***ICH9-M (5 of 5)***

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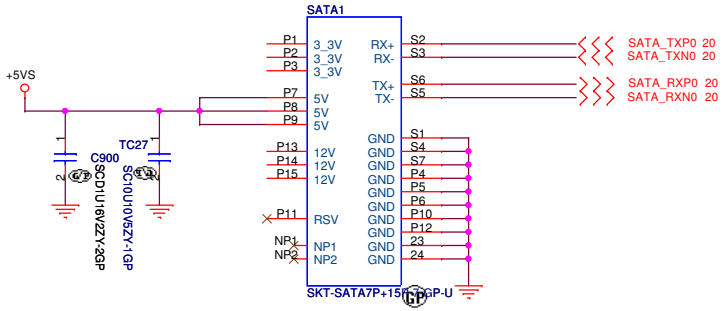
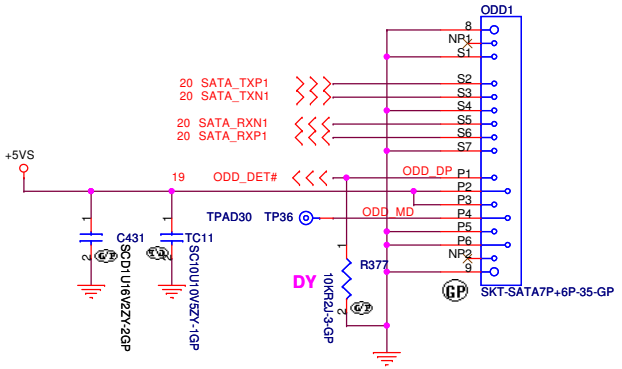
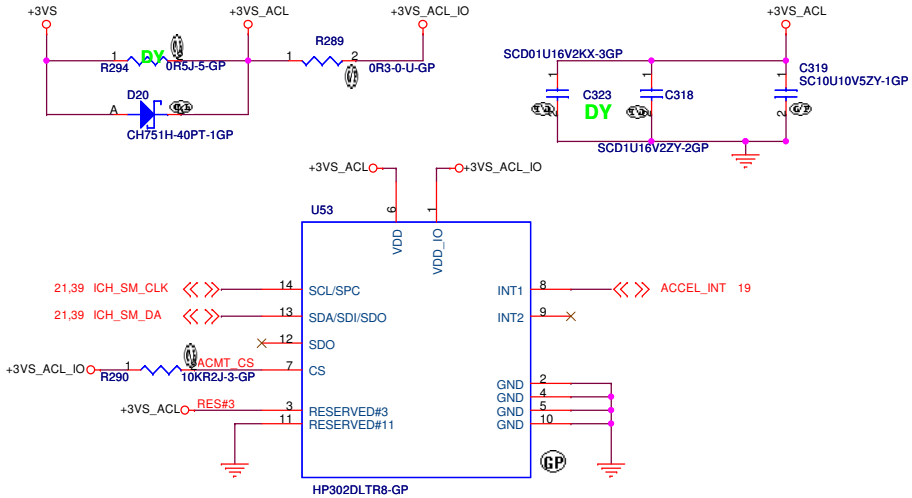
SATA HD Connector



ODD Connector



ACCELEROMETER



Must be placed in the center of the system

<Variant Name>

Wistron Corporation
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Title: HDD/ODD/ACCELEROMETER

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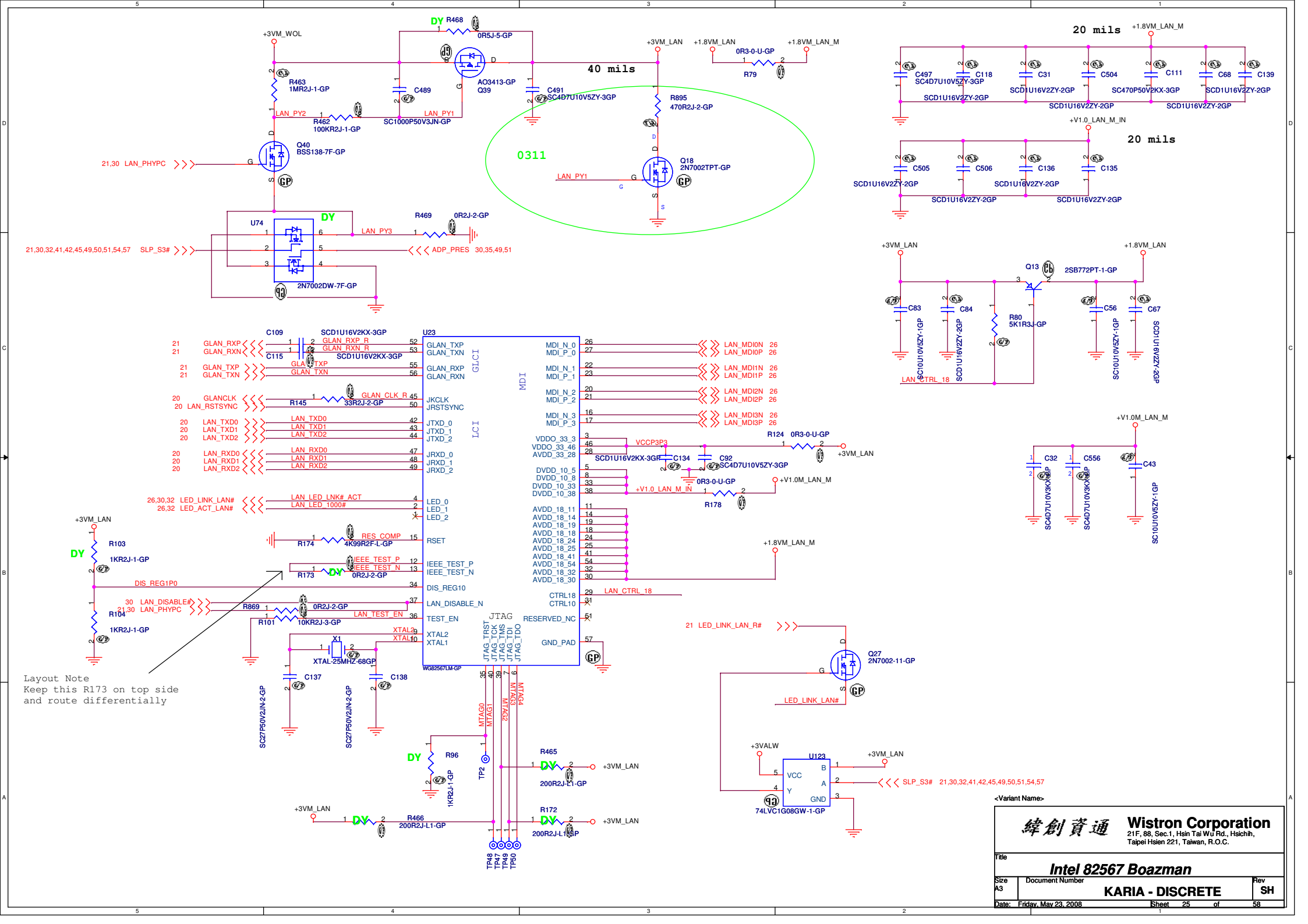
Layout Note
Keep this R173 on top side
and route differentially
0311
40 mils
20 mils
20 mils
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Intel 82567 Boazman
Size A3
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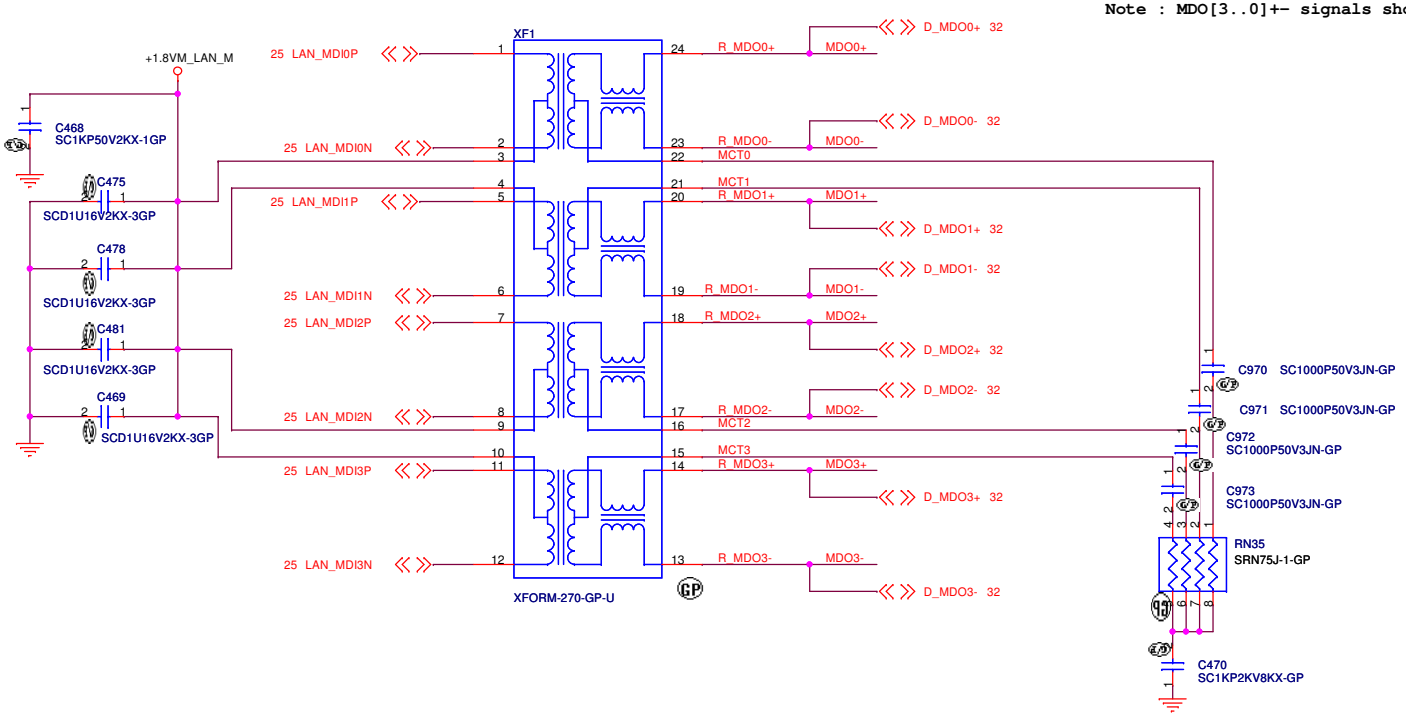
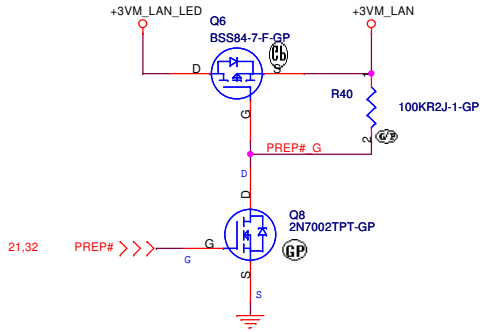
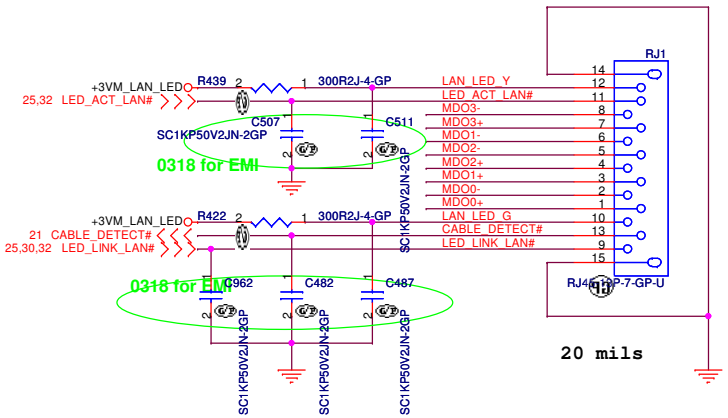
<Variant Name>

Note : MDO[3..0]+- signals should route to RJ45 first then to DOCK CONN .



LAN ENERGY DET





<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Magnetic & RJ45***

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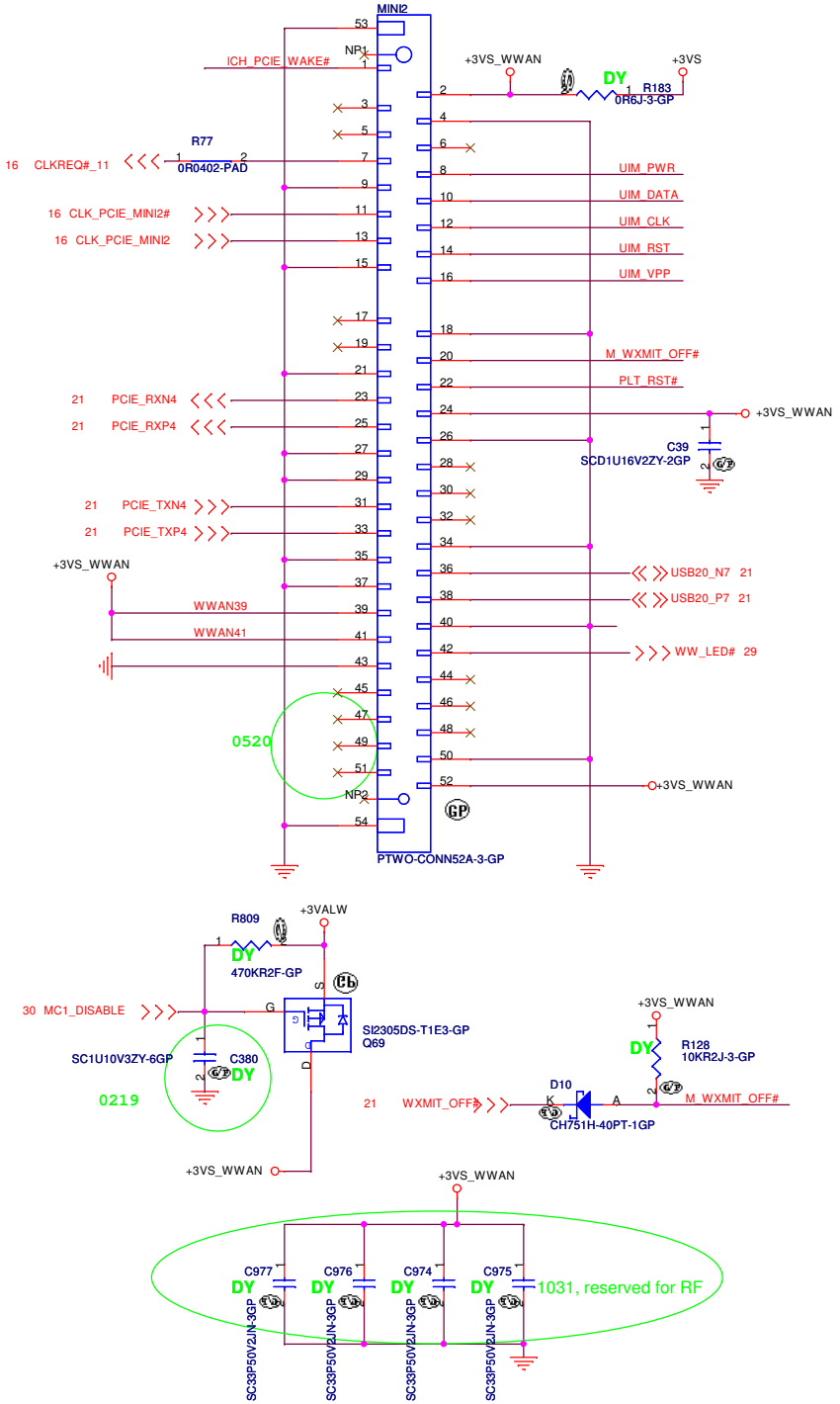
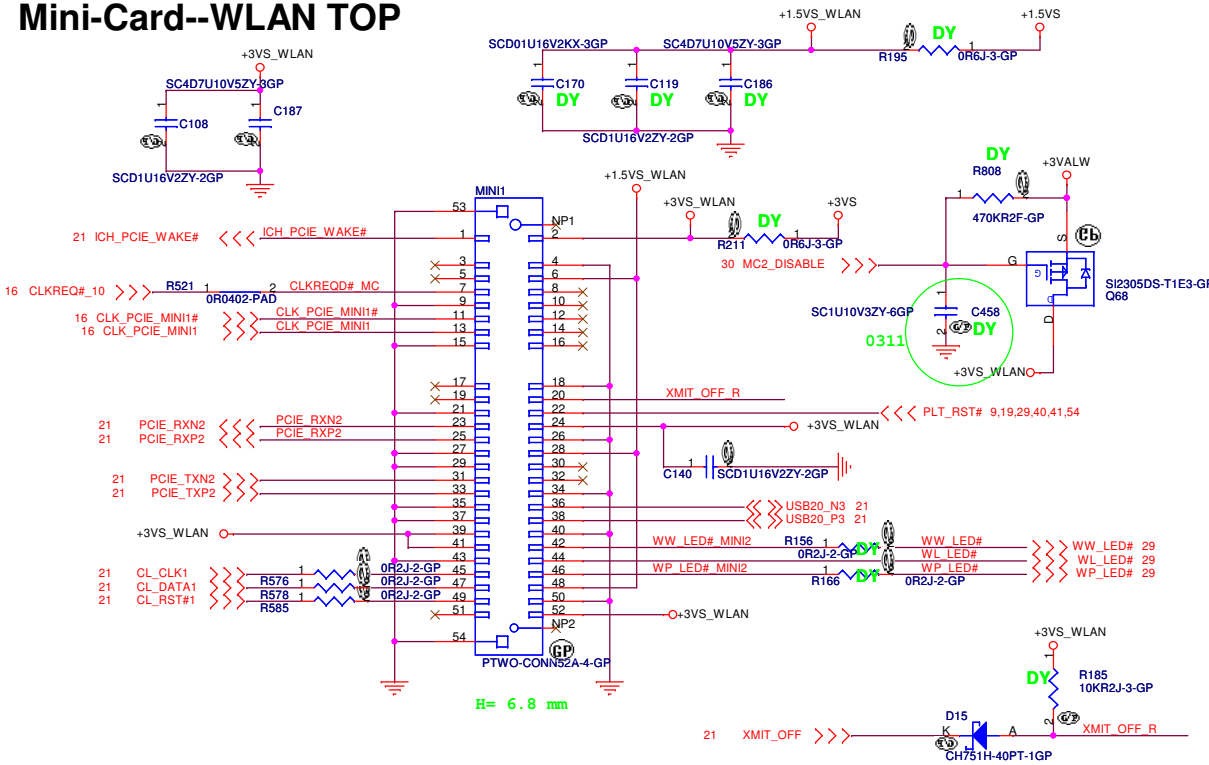
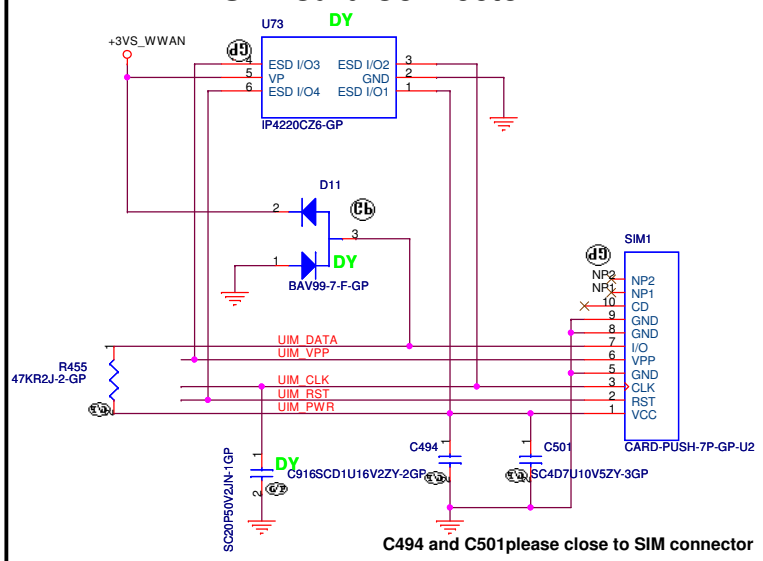
Mini-Card--WWAN BOTTOM

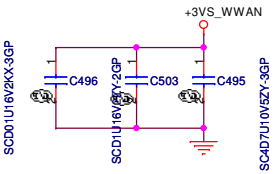


Mini-Card--WLAN TOP



Sim-Card Connector





C494 and C501please close to SIM connector

ACCELEROMETER moves to Page 24

<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Mini-Card connectors***

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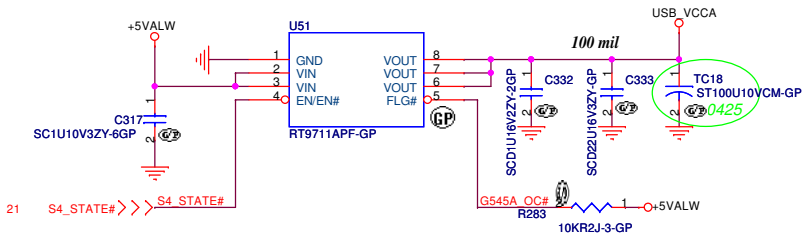

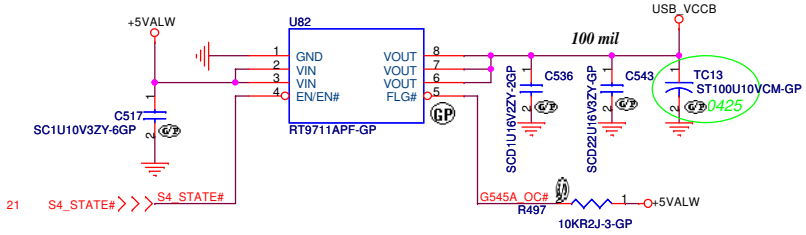

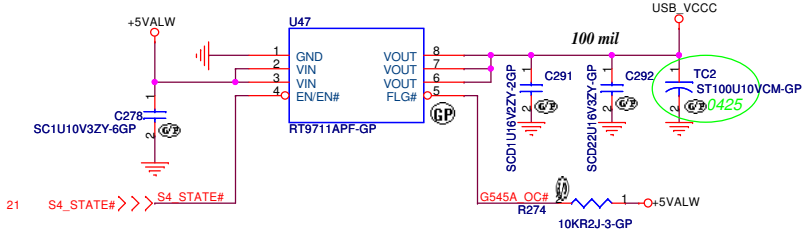

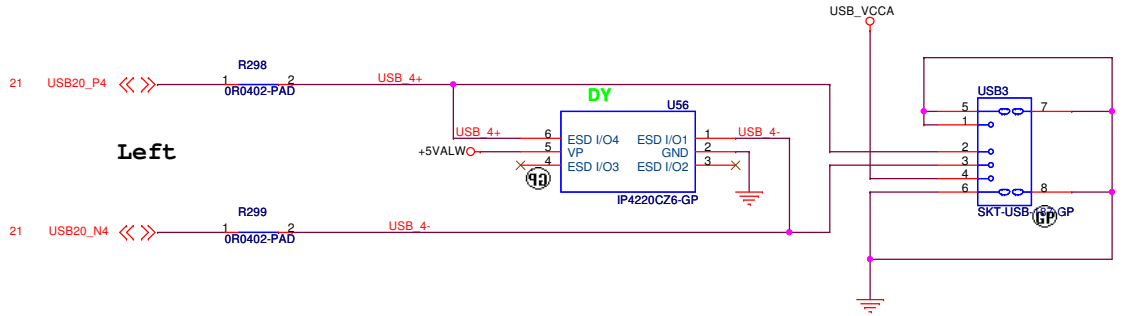

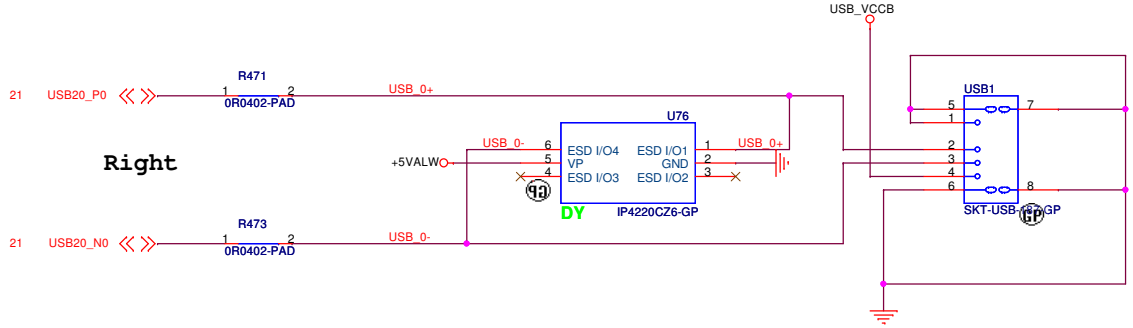

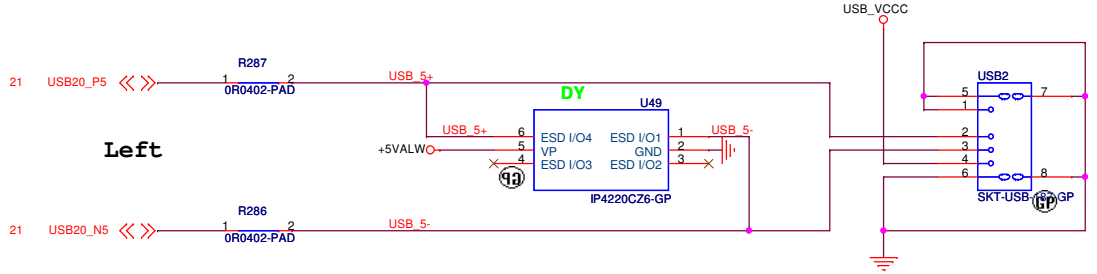

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **USB Connector**

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32Mb x 1

U86
SKT-SPI8P-GP-U
C602 SCD1U16V2ZY-2GP
30 KBC_SPI_CS0#
30 KBC_SPI_SO
R599 15R2J-GP
KBC_SPI_SO_L0
SPI_WP#
SPI_HOLD# 0
KBC_SPI_CLK 0
KBC_SPI_SI 0
R570 47R2J-2-GP
R554 47R2J-2-GP
KBC_SPI_CLK 30
KBC_SPI_SI 30
+3VL
R579 3K3R3J-L-GP
SPI_WP#
R587 0R2J-2-GP
DY
62.10076.011 & 62.10089.001
is SPI Socket part number
R550 3K3R3J-L-GP
SPI_HOLD# 0

32M SPI
> 72.25325.A01 MXIC MX25L3205D
32M SPI
> 72.26321.A01 IC FEROM AT26DF321-SU, by Atmel

Keep traces of SPI as short as possible and keep trace spacing close to 7mils to any other signal (basically follow specs).

Debug port

DEBUG1
ETY-CONN24A-GP
16 CLK_DEBUG_PORT
20,30,40 LPC_FRAME#
21,30,36,40 SIRQ
9,19,27,40,41,54 PLT_RST#
R571 0R0402-PAD
20,30,40 LPC_AD0
20,30,40 LPC_AD1
20,30,40 LPC_AD2
20,30,40 LPC_AD3
B+
30 8051TX
30 8051RX
30 8051_RECOVER#
30,33,46 VCC1_POR#_3
KBC_SPI_CLK R575 47R2J-2-GP
KBC_SPI_CS0# R600 0R0402-PAD
KBC_SPI_SI R566 47R2J-2-GP
KBC_SPI_SO R555 15R2J-GP
SPI_HOLD# 0
30 KBC_SPI_CS1#
GROUND
LPC_PCI_CLK
GROUND
LPC_FRAME#
SERIRQ
LPC_RESET#
+V3S
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
VCC_3VA
PWR_LED#
CAPS_LED#
NUM_LED#
VCC1_PWRGD
SPI_CLK
SPI_CS#
SPI_SI
SPI_SO
SPI_HOLD#
RESERVED#22
RESERVED#23
RESERVED#24
GND
GND
NP1
NP2

TPM 1.2

U71
SLB9635TT1D2-1-GP
C54 SCD1U16V2ZY-2GP
C72 SCD1U16V2ZY-2GP
C492 SCD1U16V2ZY-2GP
C485 SCD1U16V2ZY-2GP
C502 SC22P50V2JN-4GP
C509 SC18P50V2JN-1-GP
X3 X-32D768KHZ-40GPU
R477 10MR2J-L-GP
R443 4K7R2J-2-GP
R442 0R0402-PAD
R444 0R0402-PAD
R446 4K7R2J-2-GP
R445 4K7R2J-2-GP
R470 0R2J-2-GP
TPM_PP
TPM_XTALI
TPM_XTALO
9636GPIO
9636GPIO2
TP1
TP46
TPM_TESTB1
TPM_TEST1
PM_CLKRUN# 21,30,36,40
SIRQ 21,30,36,40
16 CLK_PCI_TCG
21 LPC_PD#
20,30,40 LPC_FRAME#
9,19,27,40,41,54 PLT_RST#
20,30,40 LPC_AD0
20,30,40 LPC_AD1
20,30,40 LPC_AD2
20,30,40 LPC_AD3
30 TPM_32K_CLK
VSB
VDD
XTALI/32K_IN
XTALO
LCLK
LPCPD#
LFRAME#
LRESET#
LAD0
LAD1
LAD2
LAD3
GPIO
GPIO2
TESTBI/BADD
TESTI
PP
CLKRUN#
SERIRQ
NC#1
NC#3
NC#12
GND

Mini-PCIE Card LED control circuit

PDTA114YT-GP-U
Q16
Q17
Q20
WW_LED# 27
WL_LED# 27
WP_LED# 27
41 BT_LED
R177 100KR2J-1-GP
U27
2N7002DW-7F-GP
WL_BLUE_LED# 38,41
W_LED# C
R164 100KR2J-1-GP
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPM/BIOS/24 DEBUG PORT
Size: A3
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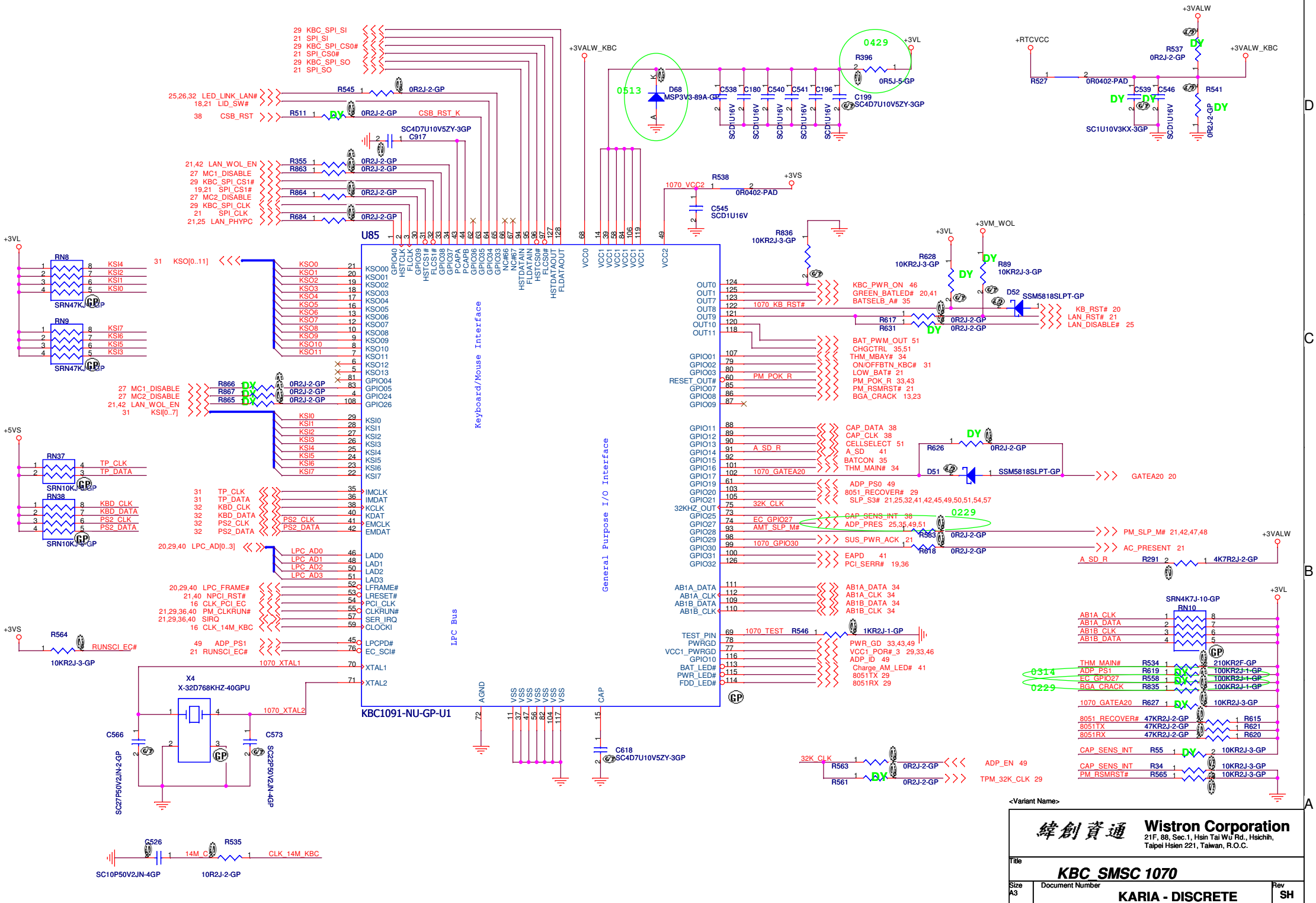
U85
KBC1091-NU-GP-U1
Keyboard/Mouse Interface
General Purpose I/O Interface
LPC Bus
X4
X-32D768KHZ-40GPU
D68
MSP3V3-89A-GP
D51
SSM5818SLPT-GP
D52
SSM5818SLPT-GP
RN8
SRN47KJ-GP
RN9
SRN47KJ-GP
RN37
SRN10KJ-GP
RN38
SRN10KJ-GP
RN10
SRN4K7J-10-GP
+3VL
+3VALW
+3VALW_KBC
+3VS
+5VS
+RTCVCC
+3VM_WOL
AGND
CAP
0429
0513
0314
0229
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
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KBC_SMSC 1070
Size
A3
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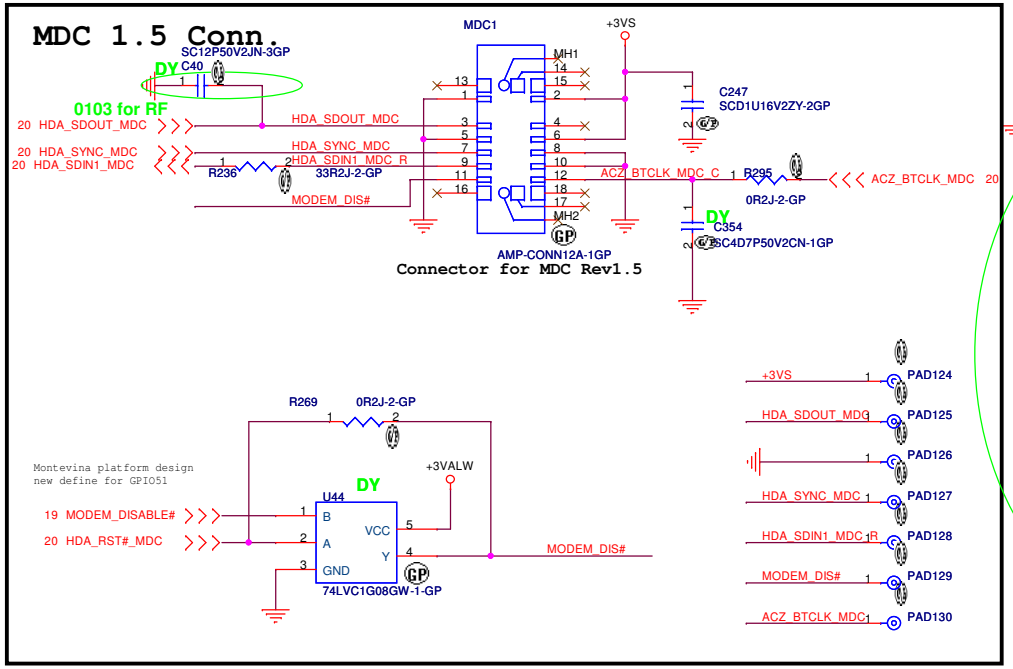

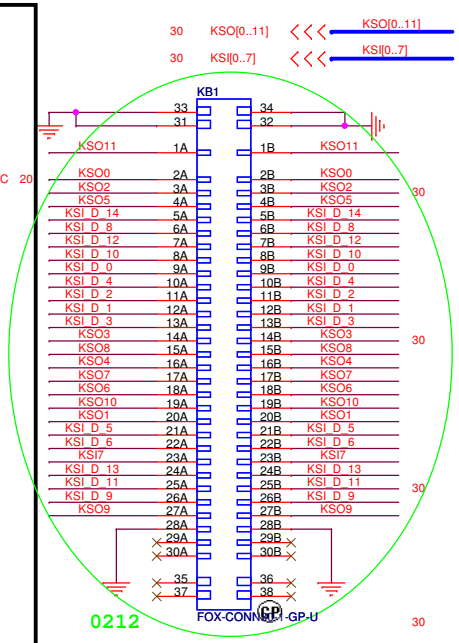

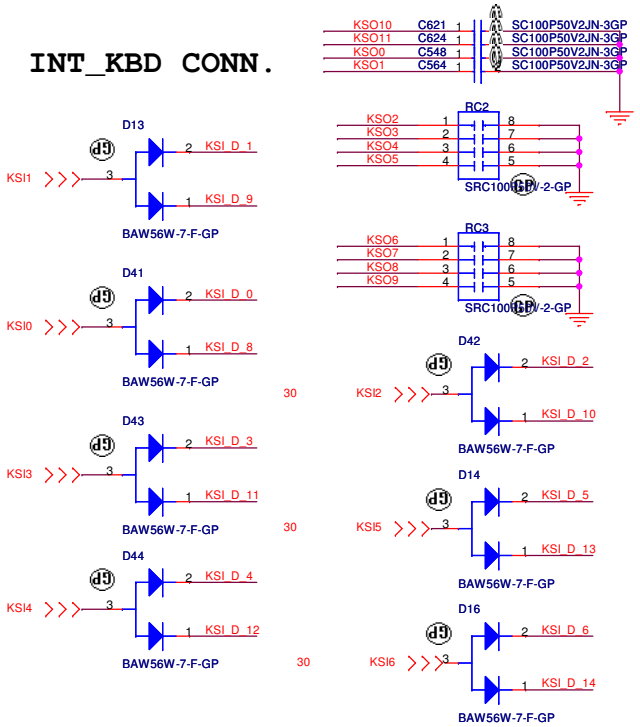

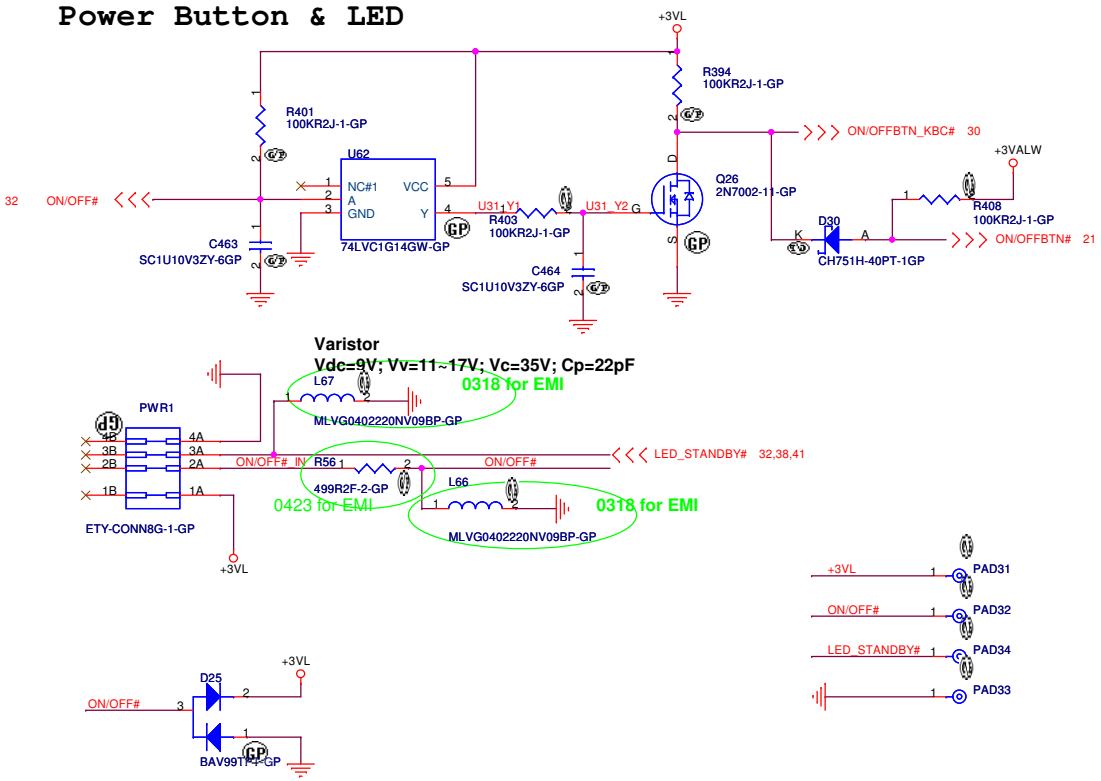

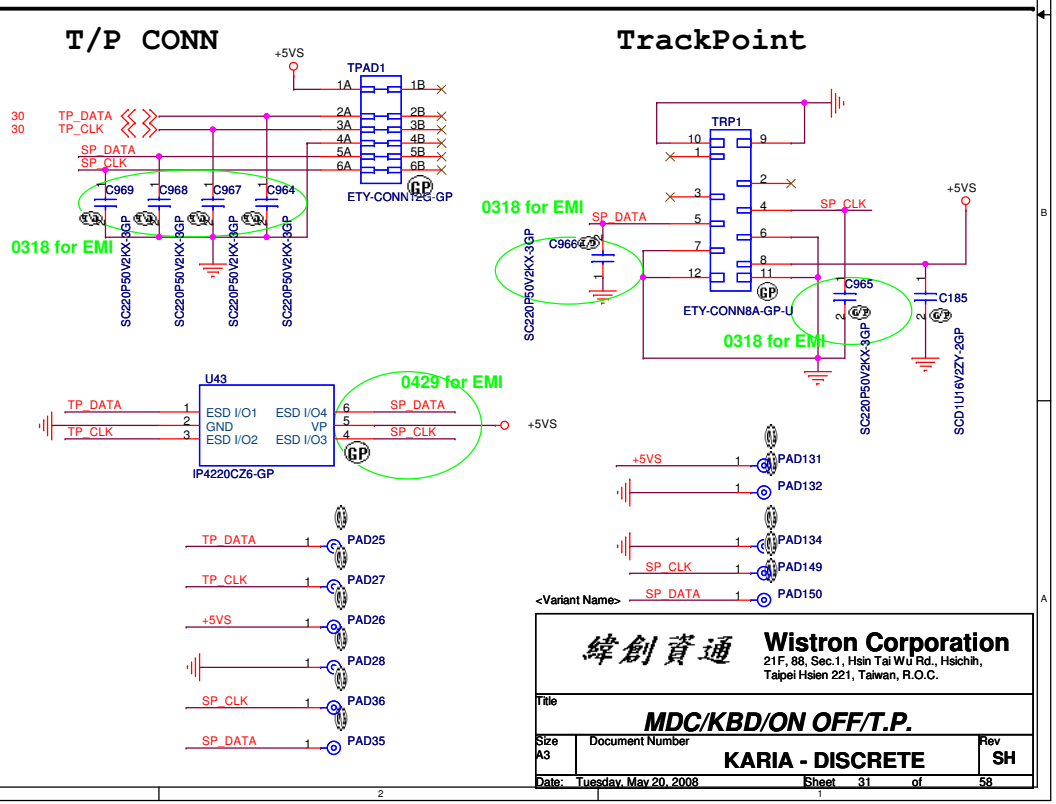

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MDC/KBD/ON OFF/T.P.***

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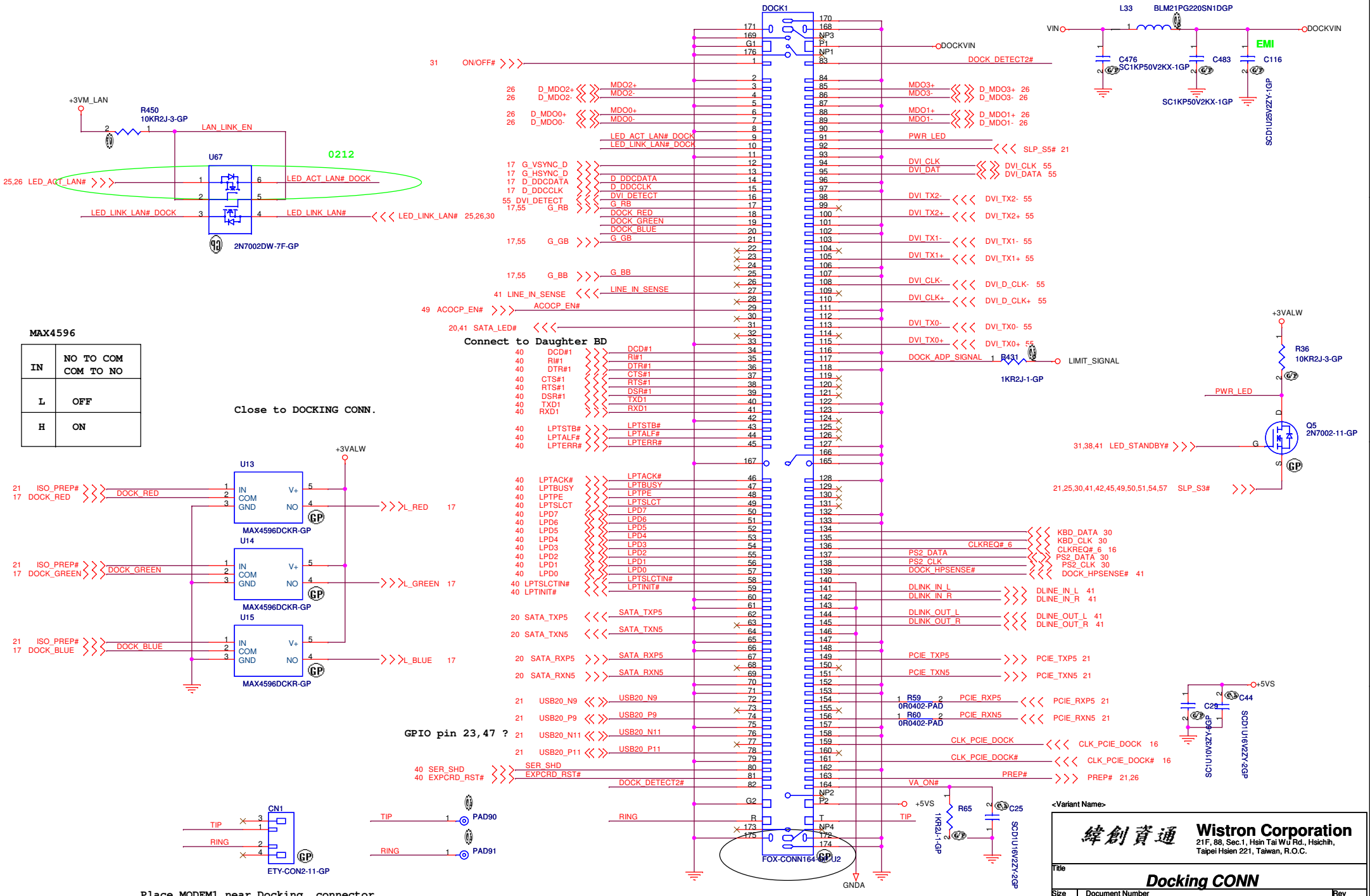
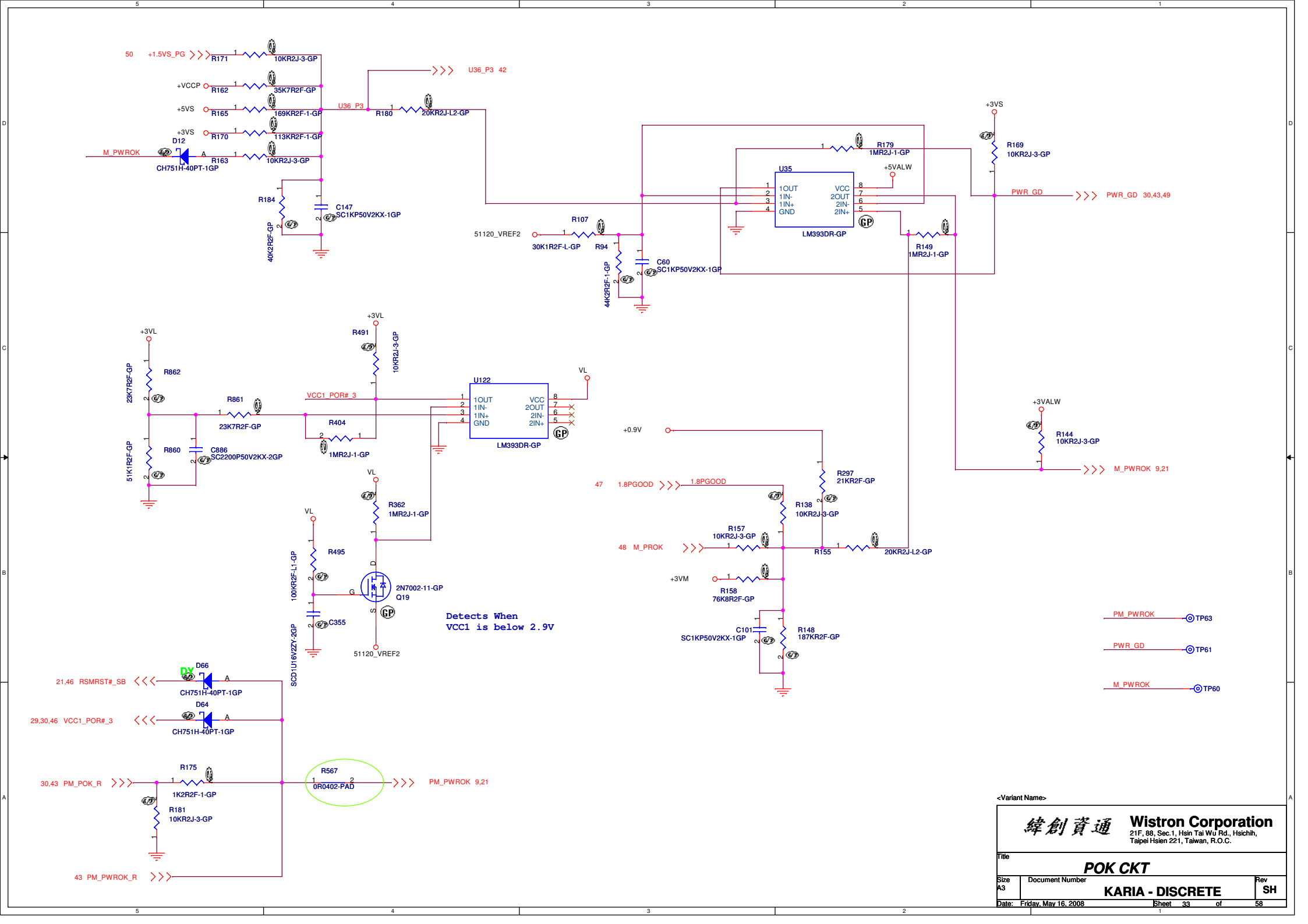
Docking CONN. 164 PIN

current rating 6A



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Docking CONN**	
Size A3	Document Number **KARIA - DISCRETE**	Rev SH
Date: Friday, May 16, 2008	Sheet 32 of 58	



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POK CKT**

Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

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Adaptor in to generate DCBATOUT

Current Rating 6 A

0423

DCIN1

SKT-JACK-190-GP

LIMIT_SIGNAL

BC2 SC1KP50V2KX-1GP

DY

ADPIN

D67 PASSMJ27APT-GP

C10 SC1KP50V2KX-1GP

VIN

R11 15KR2J-1-GP

MAIN BATTERY CONNECTOR

Current Rating 6 A

BATT_A

0318 for EMI

C37 SC1KP50V2KX-1GP

BAT1

SYN-CON8-6-GP-U1

AB1A_DATA_C

AB1A_CLK_C

OCP_ADJ_C

R61 1KR2J-1-GP

C19 SC100P50V2JN-3GP EMI

PIN 5 Voltage Feedback Circuit

D57 BAV99-5-GP

D58 BAV99-5-GP

+3VL

R71 100R2J-2-GP

R66 100R2J-2-GP

AB1A_DATA 30

AB1A_CLK 30

C33 SC100P50V2JN-3GP EMI

C36 SC100P50V2JN-3GP EMI

C38 SC220P50V2KX-3GP DY

C28 SC220P50V2KX-3GP DY

D59 BAV99-5-GP

VL

R454 69K8R2F-GP

R453 100KR2F-L1-GP

R460 294KR3F-1-GP

49 OCP_ADJ

Q37 MMBT3906-3-GP

R457 150KR2F-L-GP

R440 220KR2F-GP

Q33 2N7002-11-GP

THM_MAIN# 30

CAPS name EMI It Reserve for EMI

BATT_A PAD115

AB1A_DATA_C PAD116

AB1A_CLK_C PAD117

OCP_ADJ_C PAD118

PAD119

BAY BATTERY CONNECTOR

Current Rating 6 A

BATT_B

0318 for EMI

C102 SCD1U25V2ZY-1GP

C518 SCD01U50V2ZY-1GP

BAT2

SYN-CON8-6-GP

AB1B_DATA_C

AB1B_CLK_C

THM_MBAY#_C

D60 BAV99-5-GP

D62 BAV99-5-GP

+3VL

R116 100R2J-2-GP

R105 100R2J-2-GP

R111 210KR2F-GP

R112 1KR2J-1-GP

AB1B_DATA 30

AB1B_CLK 30

THM_MBAY# 30

C77 SC100P50V2JN-3GP EMI

C80 SC100P50V2JN-3GP EMI

C73 SC100P50V2JN-3GP EMI

D61 BAV99-5-GP

C82 SC220P50V2KX-3GP

C65 SC220P50V2KX-3GP DY

C78 SC220P50V2KX-3GP DY

BATT_B PAD120

AB1B_DATA_C PAD121

AB1B_CLK_C PAD122

THM_MBAY#_C PAD123

<Variant Name>

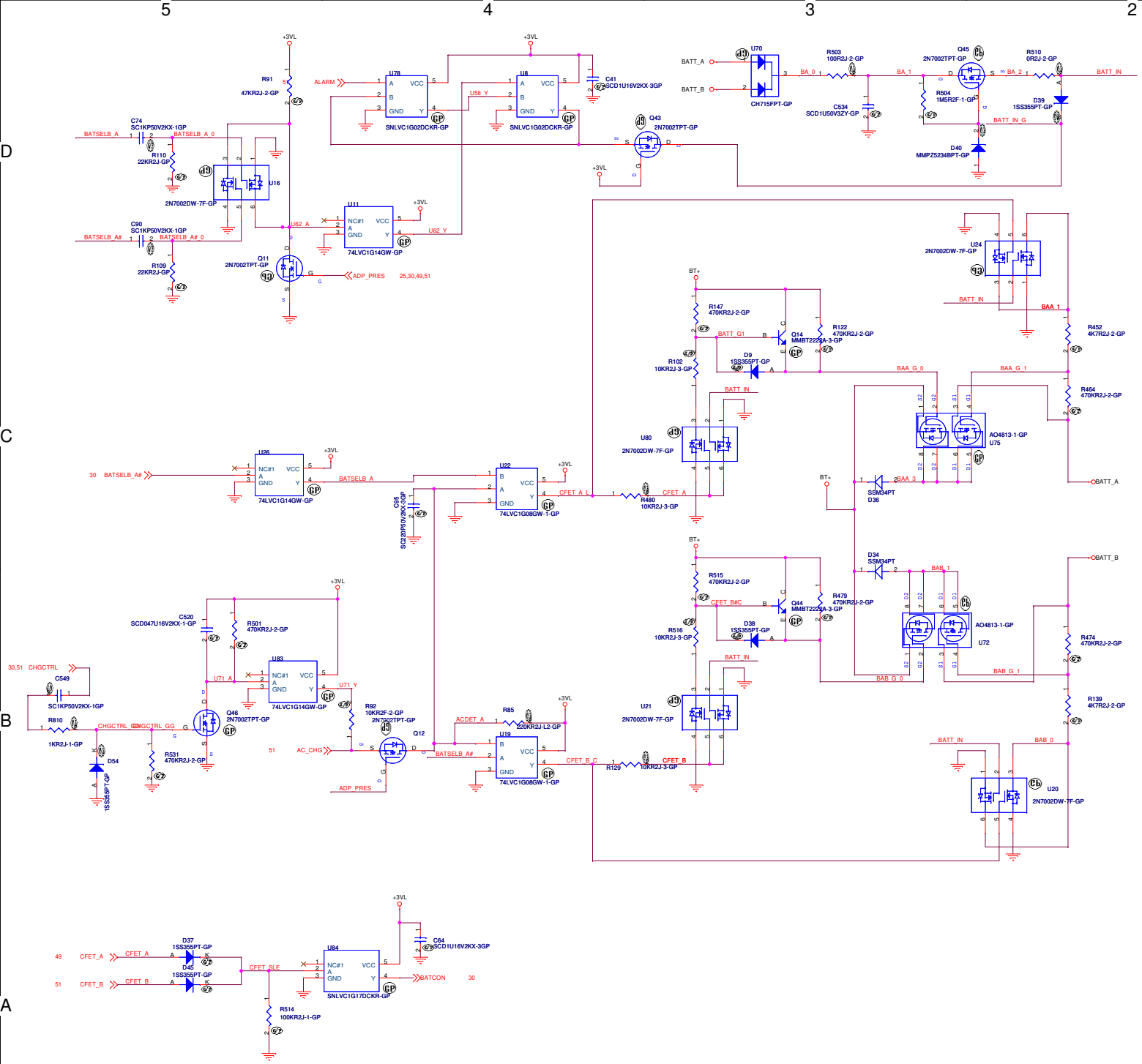
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DC & BATTERT CONN.

Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

Date: Friday, May 16, 2008 | Sheet 34 of 58



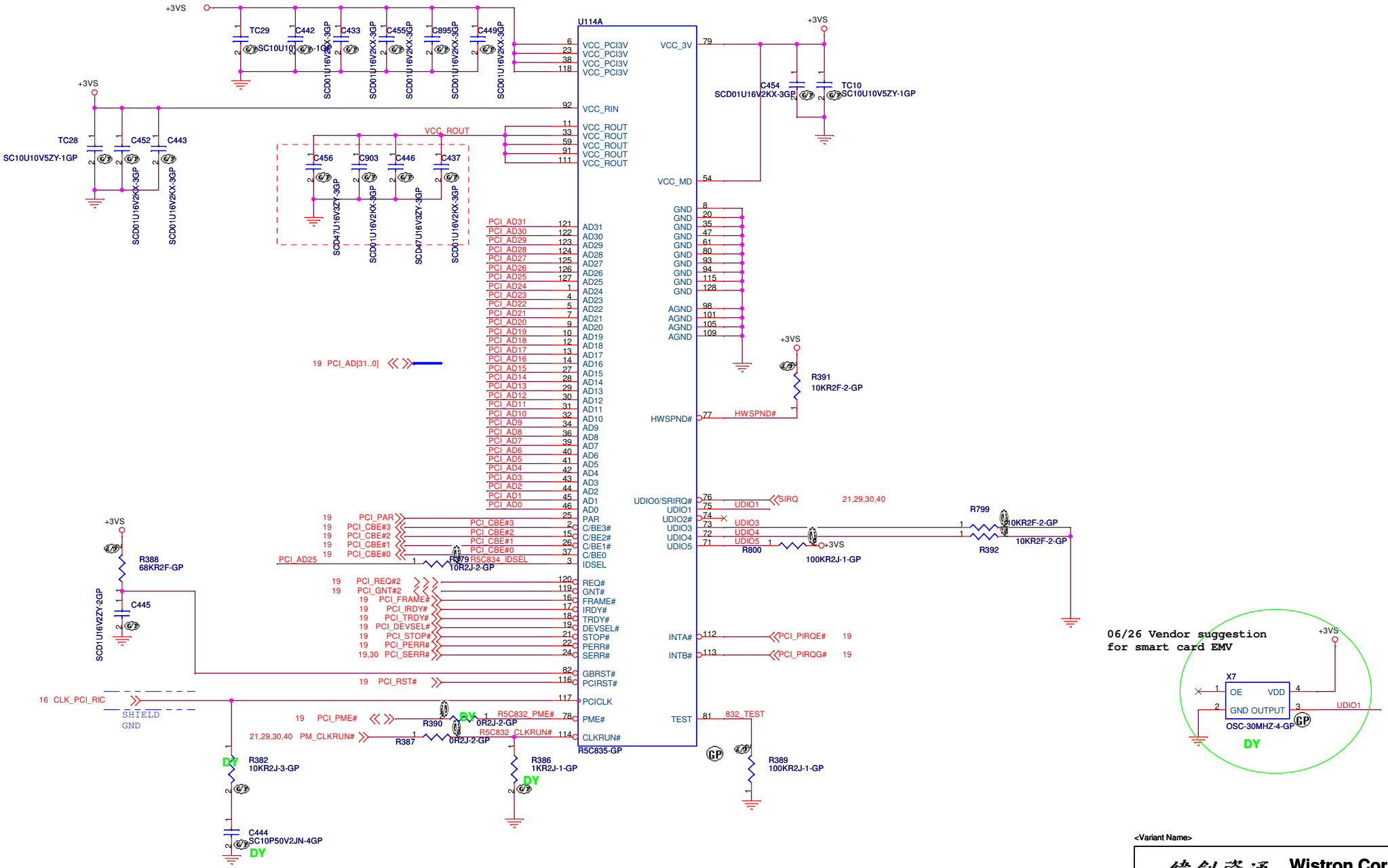
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Battery Selector***

Size	Document Number	Rev
A2	KARIA - DISCRETE	SH

Date: Monday, May 19, 2008 Sheet 35 of 58



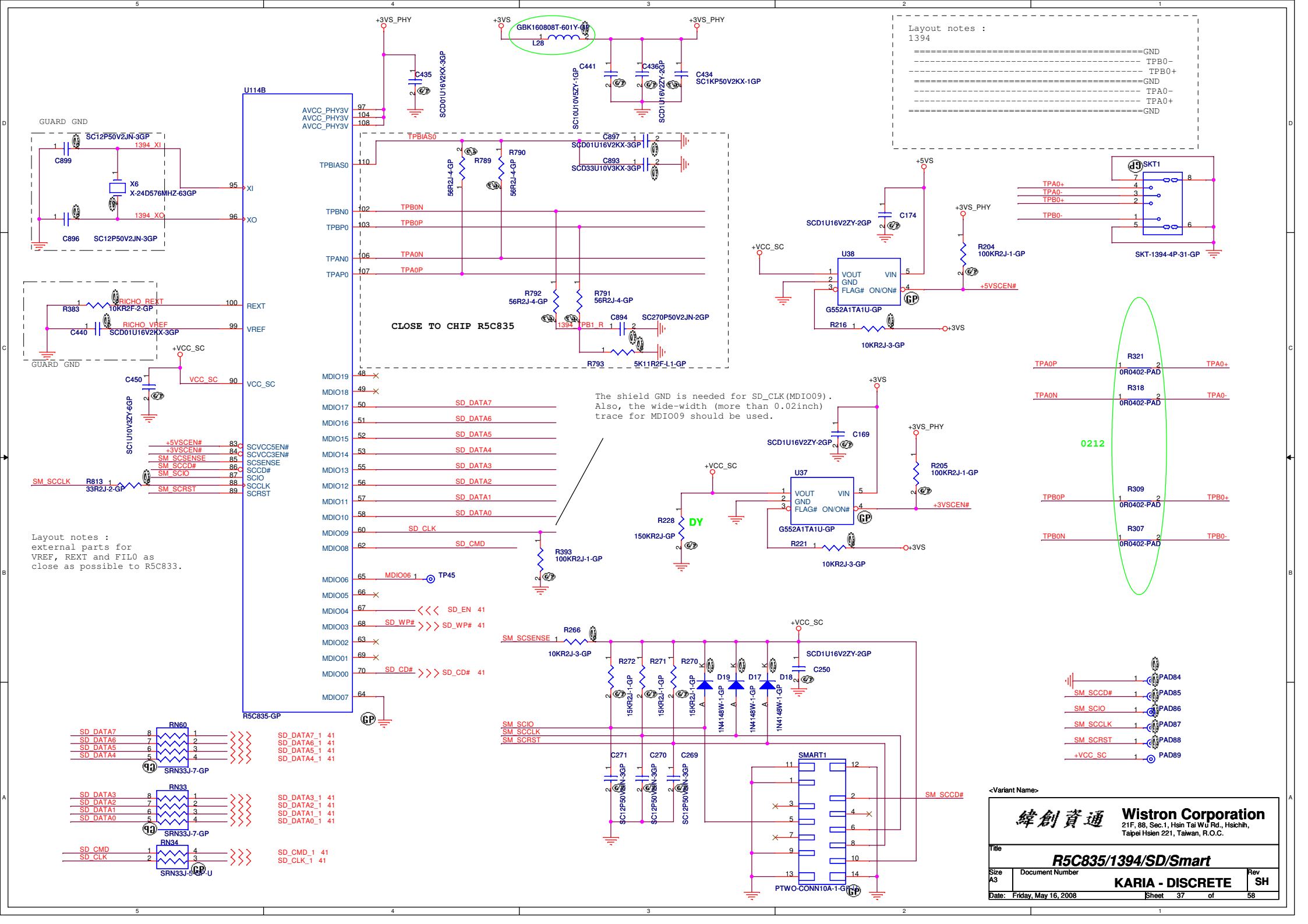
<Variant Name>

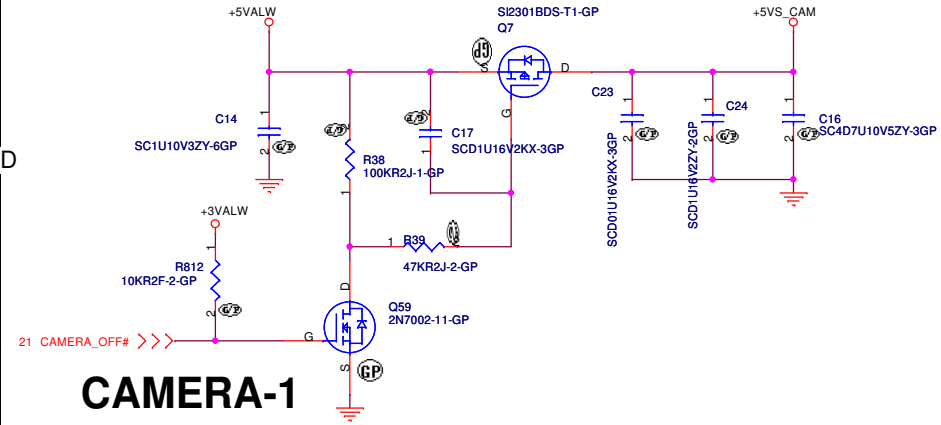
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

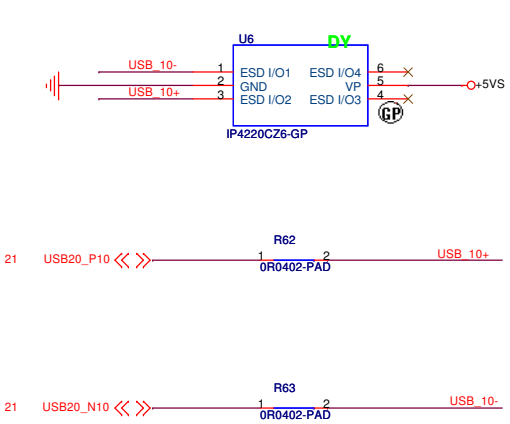
Title: R5C835/PCI

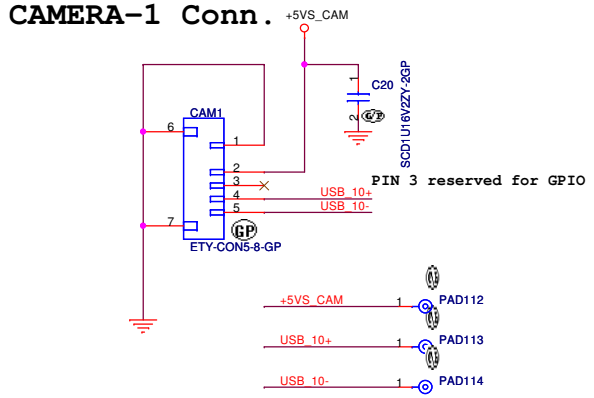
Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

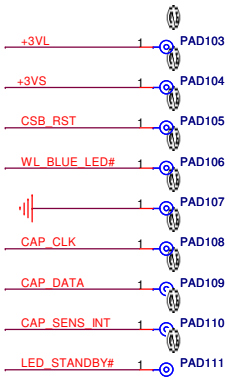
Date: Monday, May 19, 2008 | Sheet 36 of 58

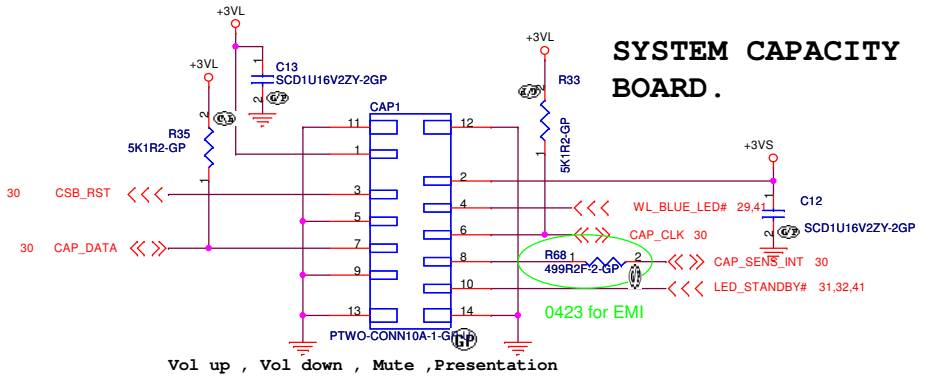

Layout notes :
1394
GND
TPB0-
TPB0+
GND
TPA0-
TPA0+
GND
U114B
R5C835-GP
CLOSE TO CHIP R5C835
The shield GND is needed for SD_CLK(MDIO09).
Also, the wide-width (more than 0.02inch)
trace for MDIO09 should be used.
Layout notes :
external parts for
VREF, REXT and FIL0 as
close as possible to R5C833.
SKT1
SKT-1394-4P-31-GP
G552A1TA1U-GP
SMART1
PTWO-CONN10A-1-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
R5C835/1394/SD/Smart
KARIA - DISCRETE
Date: Friday, May 16, 2008
Sheet 37 of 58

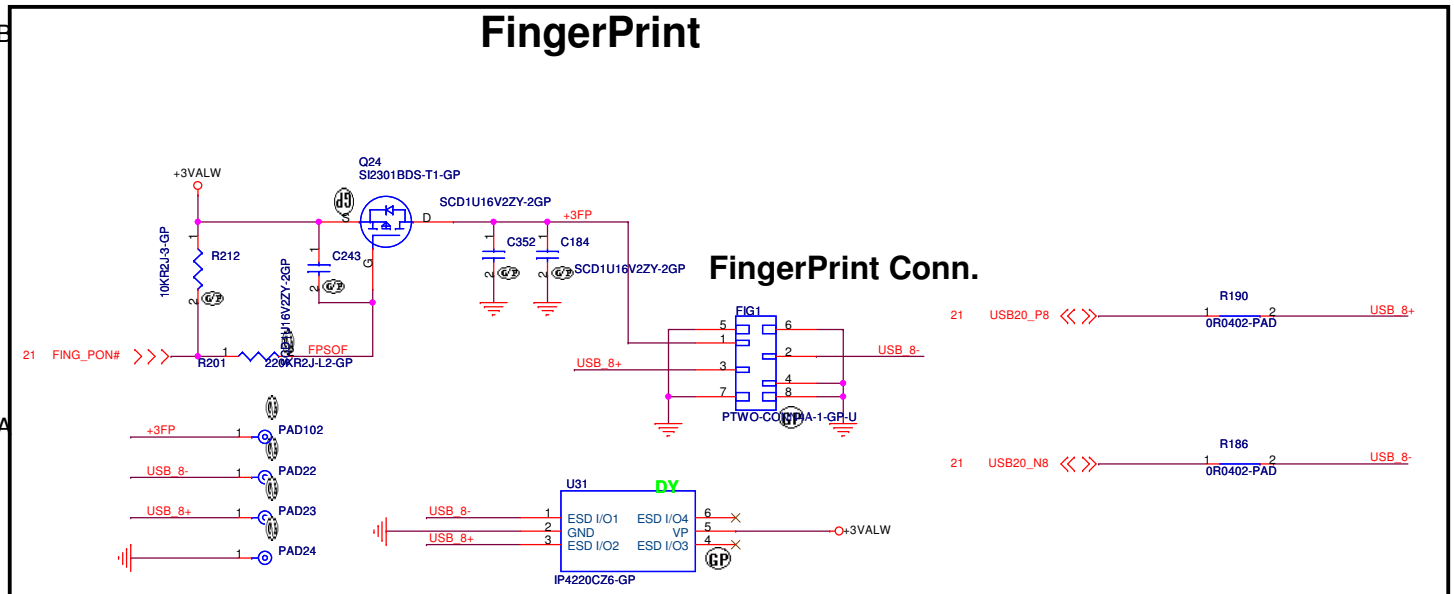


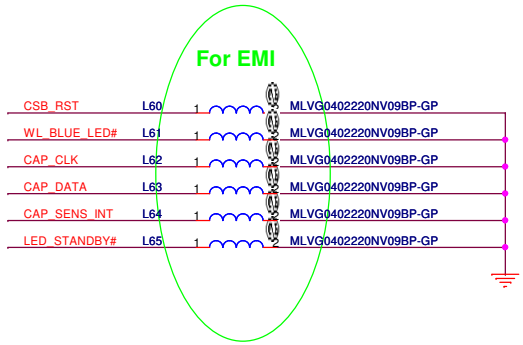












<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Camera/W-COM

Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

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CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near thermal diode

5 H_THERMDA — SC22P50V2JN-4GP C349 — H_THERMDA

CLOSE TO CPU

DY

5 H_THERMDC — H_THERMDC

55 GPU_TEMP+ — SC22P50V2JN-4GP C522 — GPU_TEMP+

DY

55 GPU_TEMP- — GPU_TEMP-

GPU DIE TEMP:
REMOTE2+ and REMOTE2- routing 10mil trace width and 10 mil spacing.

D1+ C788 1 — SC100P50V2JN-3GP — D1-

D2+ C782 1 — SC100P50V2JN-3GP — D2-

CLOSE TO BMC2103

R811 49D9R2F-GP +3VS — SCD1U16V2KX-3GP C751

U106 EMC2103-2-AP-GP

VDD, DP1, DN1, DP2/DN3, ND2/DP3, SYS_SHDN#, ALERT#, SMCLK, SMDATA, GPIO1, GPIO2, TACH, PWM, TRIP_SET, SHDN_SEL, GND, GND

R206 10KR2J-3-GP +3VS

H_THERMDA R733 0R2J-2-GP D1+
H_THERMDC R732 0R2J-2-GP D1-
GPU_TEMP+ R719 0R2J-2-GP D2+
GPU_TEMP- R720 0R2J-2-GP D2-

1017

SYS_SHDN#

21,55 THERM_SCI# — THERM_SCI# R R686 0R2J-2-GP

21,24 ICH_SM_CLK
21,24 ICH_SM_DA

THERMTRIP#1 — TP67

FAN_TACH

0526 R712 1K5R2F-2-GP

R710 15KR2F-GP 0311

+3VS R729 10KR2J-3-GP — FAN_TACH 5

+3VS R701 10KR2J-3-GP — FAN_PWM 5

R848 0R2J-2-GP — PM_THRMTRIP-A# 5,9,20

+3VS R310 10KR2J-3-GP DY — Q70 RHU002N06-1-GP DY

+3VS R268 10KR2J-3-GP DY

SYS_SHDN# — Q71 RHU002N06-1-GP DY

G_TEMP_FAIL# R850 0R2J-2-GP

Q58 2N7002TPT-GP — G_TEMP_FAIL 55

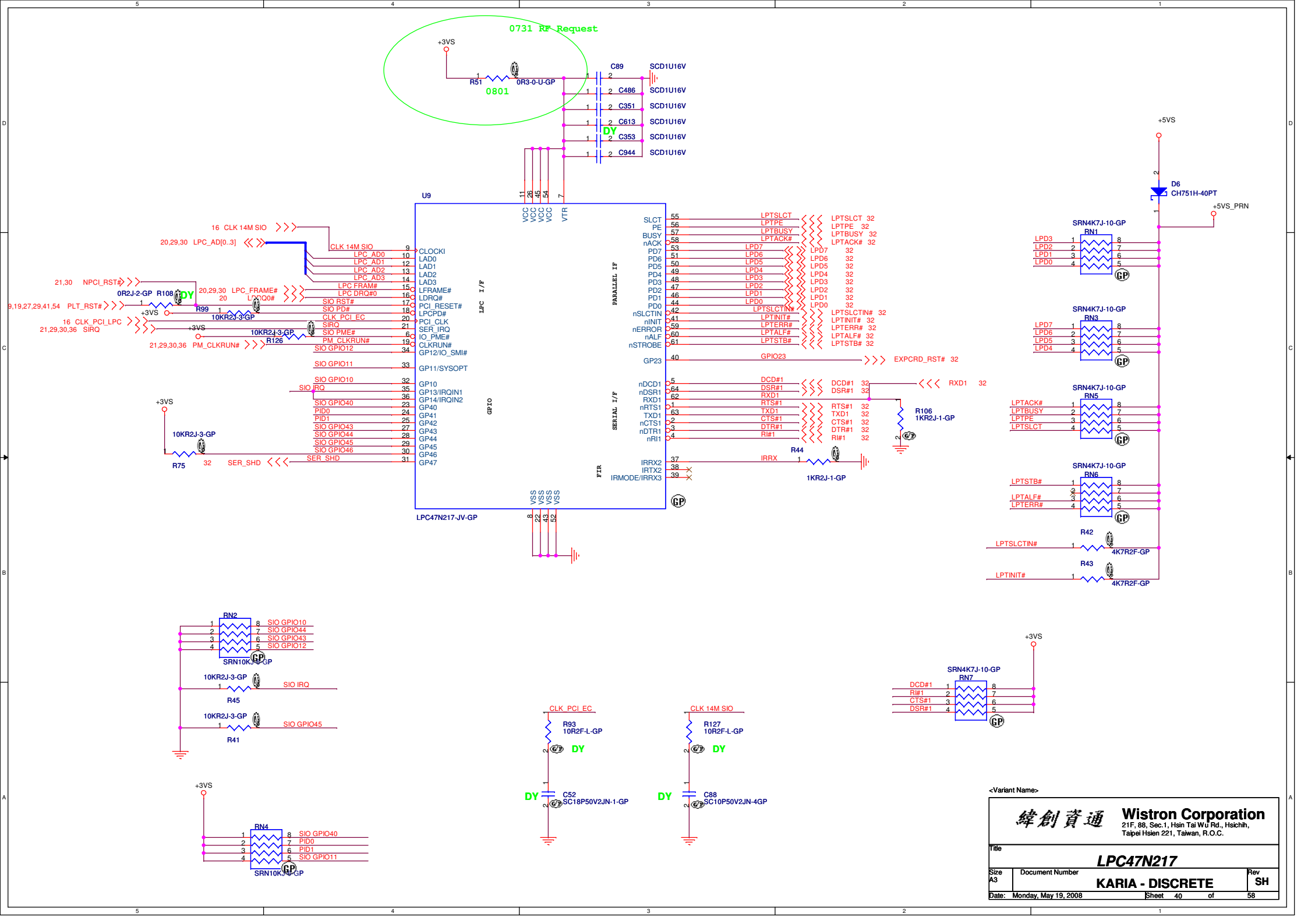
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADT7473 Thermal Sensor

Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

Date: Monday, May 26, 2008 Sheet 39 of 58


0731 RF Request
0801
U9
LPC47N217-JV-GP
LPC I/F
GPIO
PARALLEL IF
SERIAL I/F
FIR
+3VS
+5VS
+5VS_PRN
D6
CH751H-40PT
R51
0R3-0-U-GP
C89
SCD1U16V
C486
C351
C613
C353
C944
DY
SRN4K7J-10-GP
RN1
RN3
RN5
RN6
RN7
RN2
RN4
SRN10KJ-GP
R42
R43
4K7R2F-GP
R44
1KR2J-1-GP
R106
1KR2J-1-GP
R75
R45
R41
10KR2J-3-GP
R99
10KR2J-3-GP
R126
10KR2J-3-GP
R108
0R2J-2-GP
R93
10R2F-L-GP
R127
10R2F-L-GP
C52
SC18P50V2JN-1-GP
C88
SC10P50V2JN-4GP
CLK 14M SIO
CLK_PCI_EC
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC FRAM#
LPC DRQ#0
SIO RST#
SIO PD#
CLK_PCI_EC
SIRQ
SIO PME#
PM_CLKRUN#
SIO GPIO12
SIO GPIO11
SIO GPIO10
SIO IRQ
SIO GPIO40
PID0
PID1
SIO GPIO43
SIO GPIO44
SIO GPIO45
SIO GPIO46
SER_SHD
LPTSLCT
LPTPE
LPTBUSY
LPTACK#
LPTERR#
LPTALF#
LPTSTB#
LPTINIT#
LPTSLCTIN#
GPIO23
EXPCRD_RST# 32
RXD1 32
IRRX
NPCI_RST#
PLT_RST#
LPC_AD[0..3]
LPC_FRAME#
LPC_DRQ0#
SER_IRQ
IO_PME#
PM_CLKRUN#
SIRQ
CLK_PCI_LPC
SER_SHD
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LPC47N217
Size A3
Document Number
KARIA - DISCRETE
Rev SH
Date: Monday, May 19, 2008
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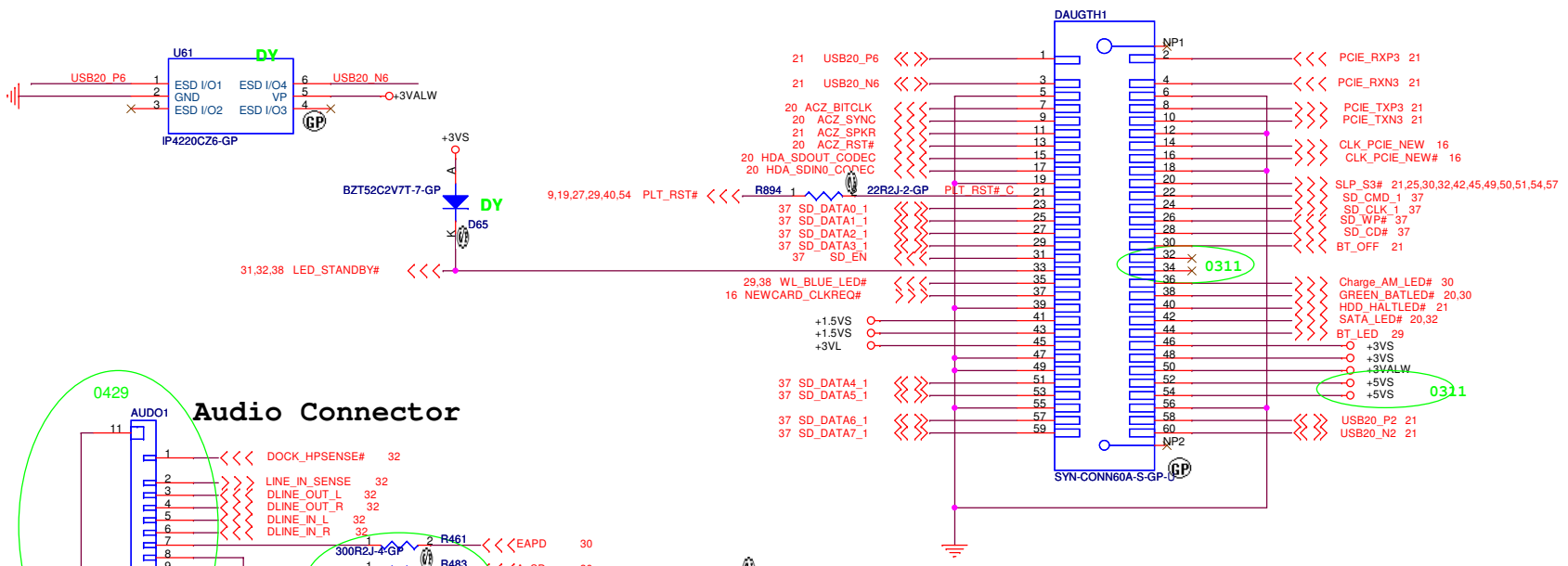
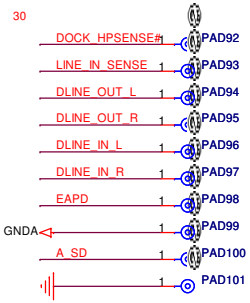
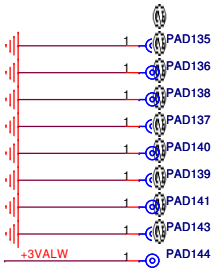
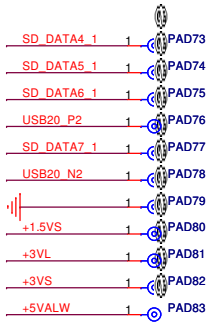
Daughter Board Connector

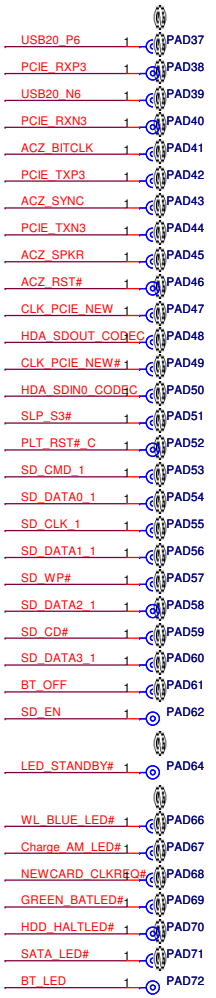


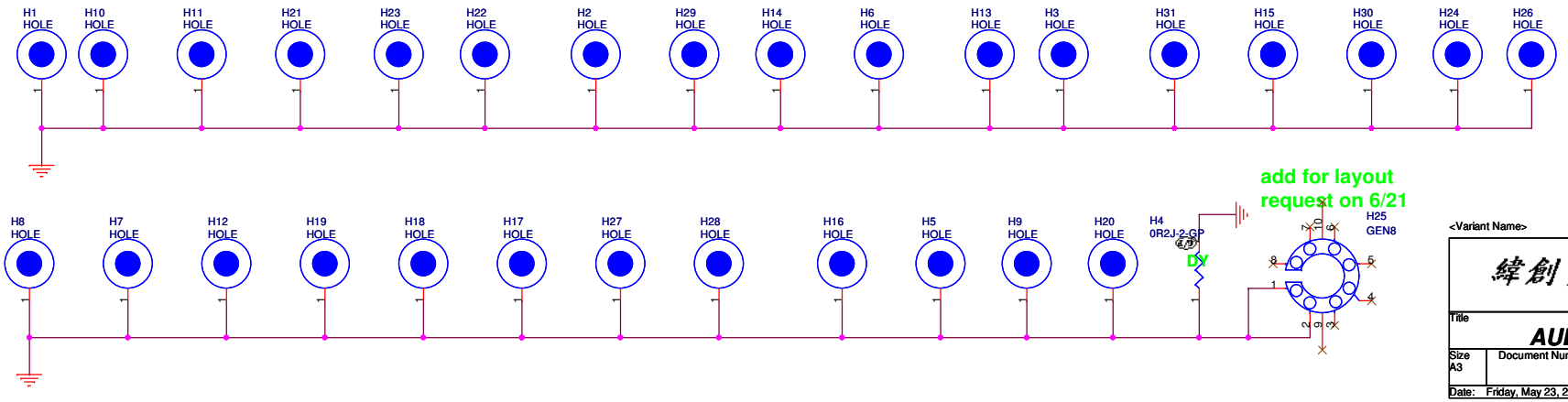
Audio Connector

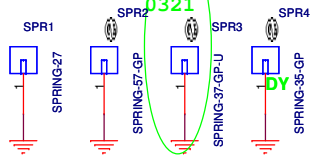












H10,H5 P/N: 34.4V908.001
H27,H28 P/N: 34.4V909.001
H9,H13 P/N:34.4V907.001
H21 P/N:34.4V910.001

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDO/Daughter Connector

Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

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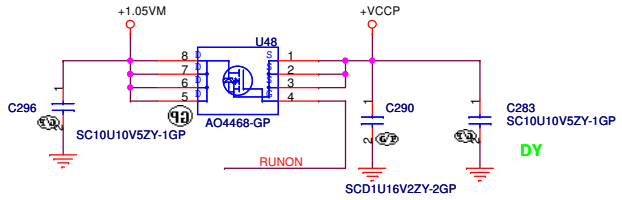
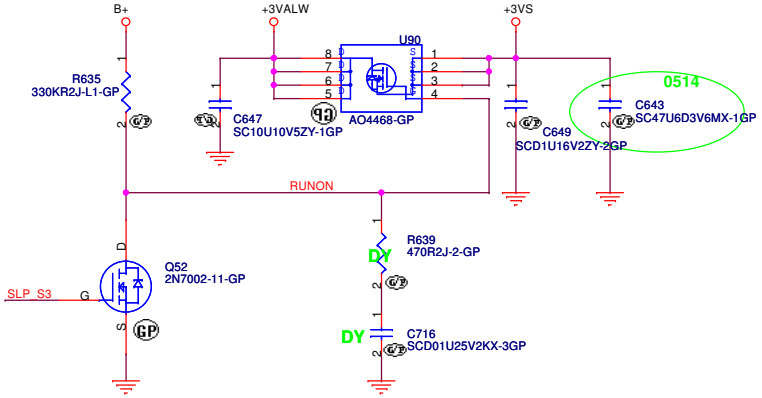
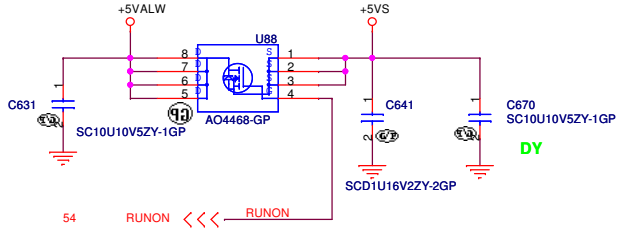
+1.05VM to +VCCP Transfer



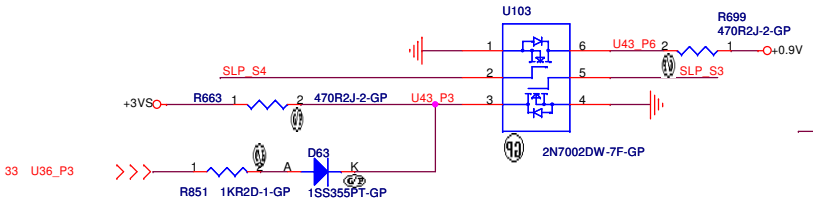
+3VALW to +3VS Transfer



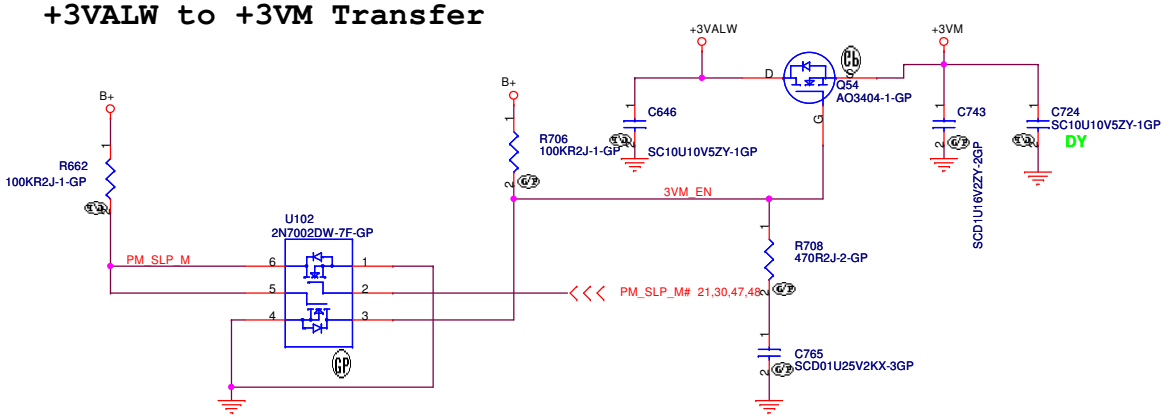
+5VALW to +5VS Transfer



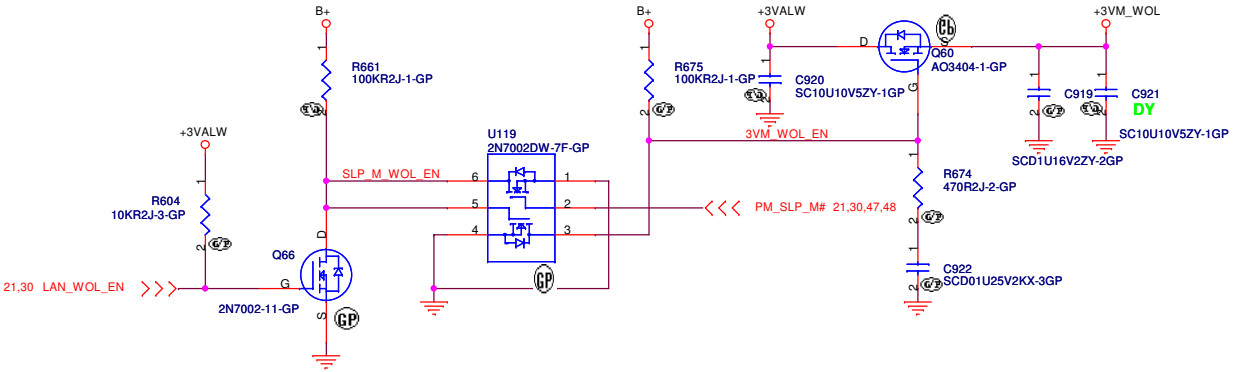
Discharge circuit-1



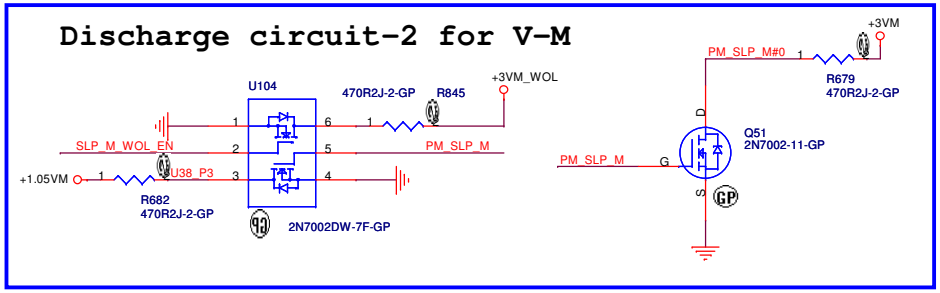
+3VALW to +3VM Transfer

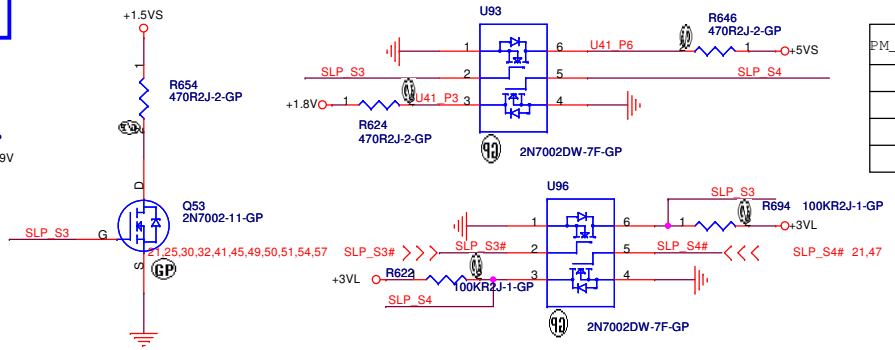


+3VALW to +3VM_WOL



Discharge circuit-2 for V-M





PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM	SYSTEM STATE
0	0	0V	0V	Moff / No WOL
0	1	3.3V	0V	Legacy WOL/ Moff
1	0	3.3V	3.3V	M1
1	1	3.3V	3.3V	M1

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC Circuit

Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

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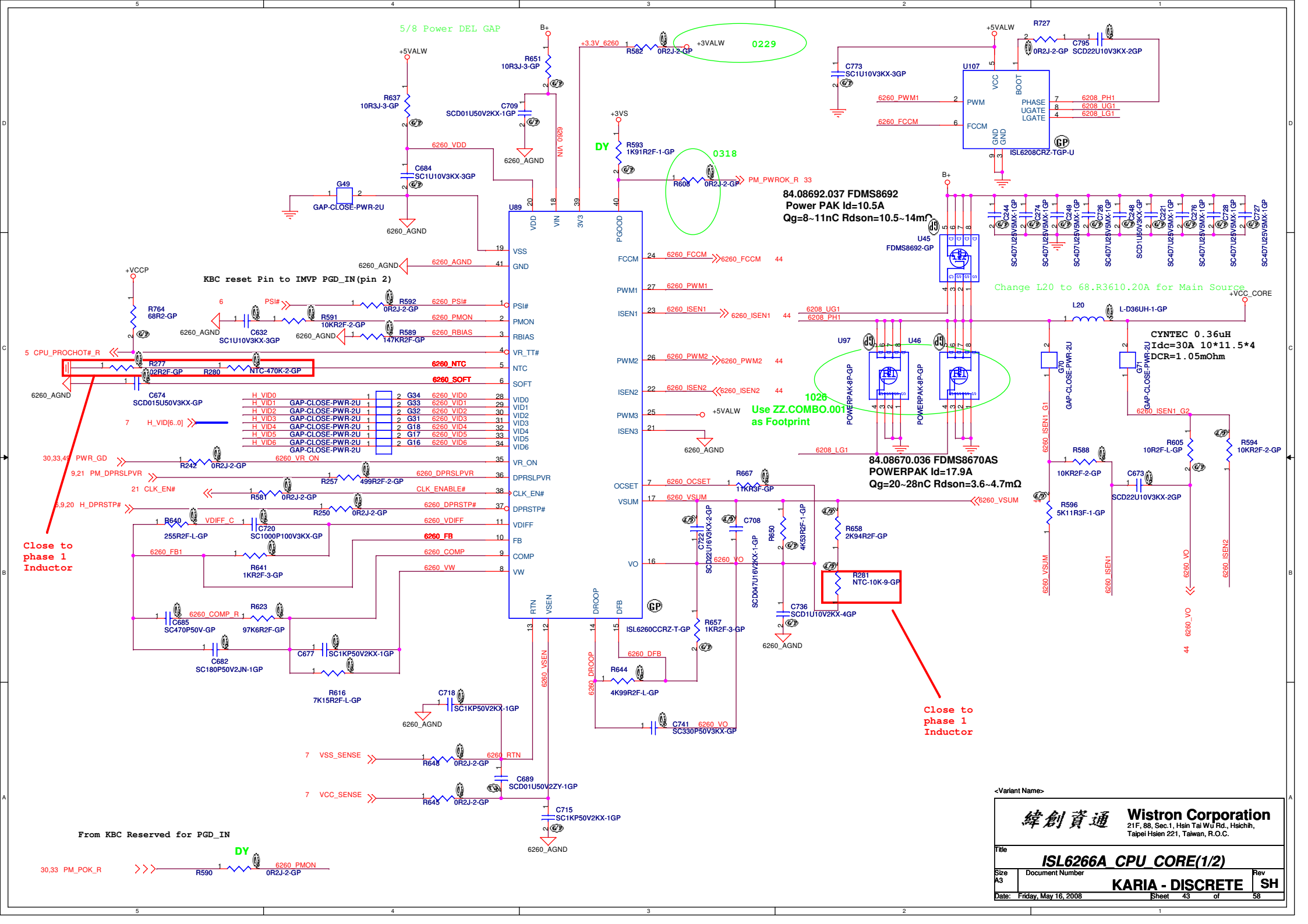
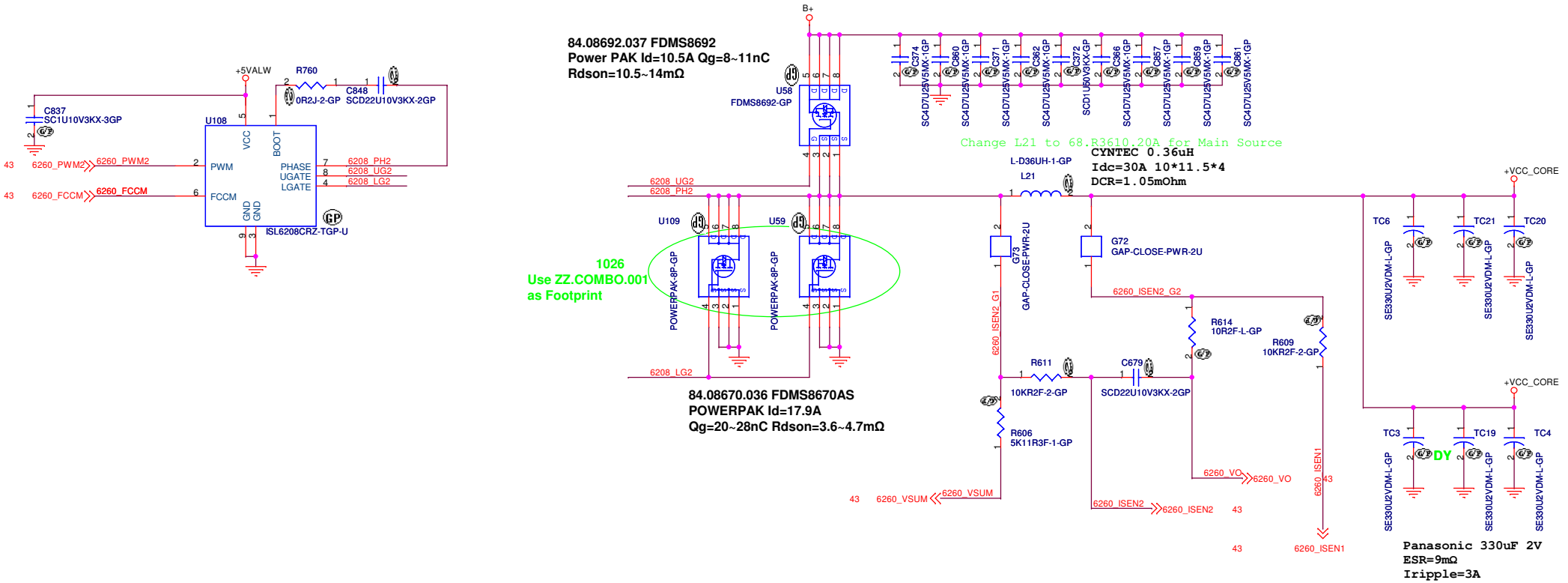
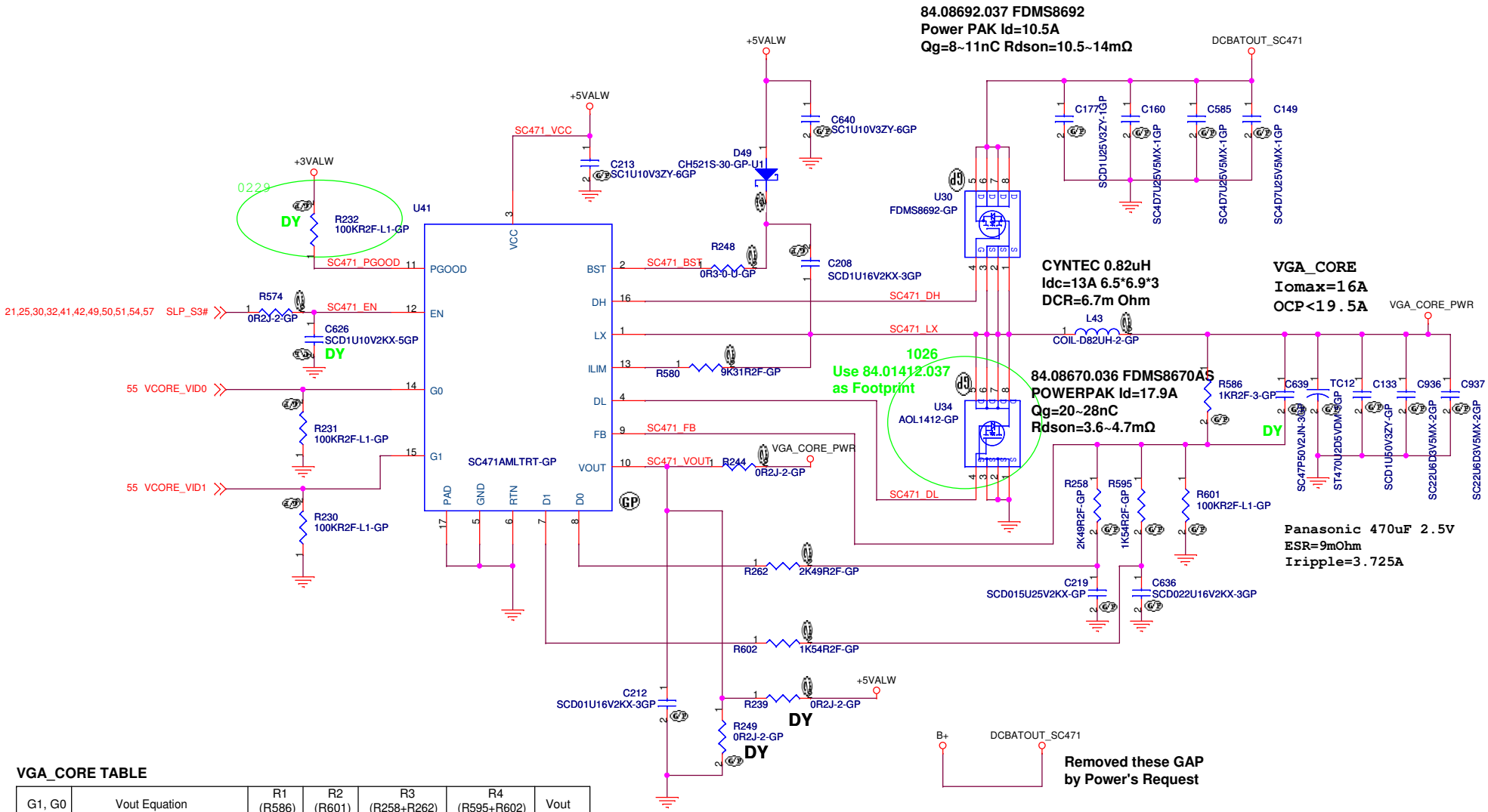

5/8 Power DEL GAP
KBC reset Pin to IMVP PGD_IN(pin 2)
84.08692.037 FDMS8692
Power PAK Id=10.5A
Qg=8~11nC Rdson=10.5~14mΩ
84.08670.036 FDMS8670AS
POWERPAK Id=17.9A
Qg=20~28nC Rdson=3.6~4.7mΩ
Change L20 to 68.R3610.20A for Main Source
CYNTEC 0.36uH
Idc=30A 10*11.5*4
DCR=1.05mOhm
Use ZZ.COMBO.001
as Footprint
Close to phase 1 Inductor
Close to phase 1 Inductor
From KBC Reserved for PGD_IN
ISL6266A_CPU_CORE(1/2)
Wistron Corporation
KARIA - DISCRETE



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***ISL6266A_CPU_CORE(2/2)***
Size A3 / Document Number	**KARIA - DISCRETE** / Rev **SH**
Date: Monday, May 19, 2008	Sheet 44 of 58



VGA_CORE TABLE

G1, G0	Vout Equation	R1 (R586)	R2 (R601)	R3 (R258+R262)	R4 (R595+R602)	Vout
(0,0)	0.75*(1+R1/R2+R1/R3+R1/R4)	1K	100K	4.98K	3.82K	1.104V
(0,1)	0.75*(1+R1/R2+R1/R4)	1K	100K		3.08K	1.001V
(1,0)	0.75*(1+R1/R2+R1/R3)	1K	100K	4.98K		0.908V
(1,1)	0.75*(1+R1/R2)	1K	100K			0.758V

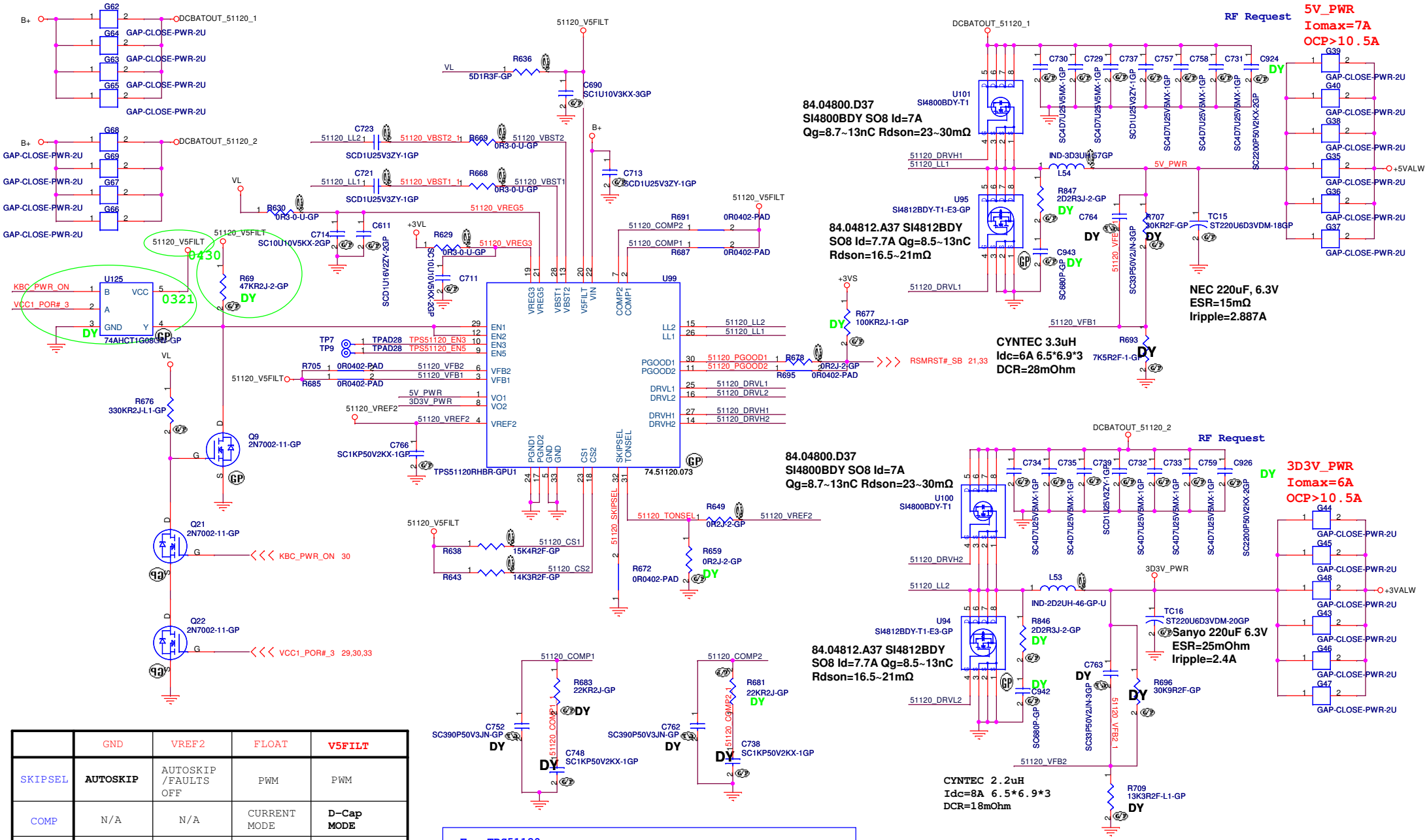
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SC471A_VGA CORE**

Size: B | Document Number: **KARIA - DISCRETE** | Rev: SH

Date: Friday, May 16, 2008 | Sheet 45 of 58



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	Adjustable output (connect to the resistor divider)			**5V Fixed Output**
VFB2				**3.3V Fixed Output**
EN1,EN2	Switcher OFF		**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on (EN3 only)

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Variant Name>

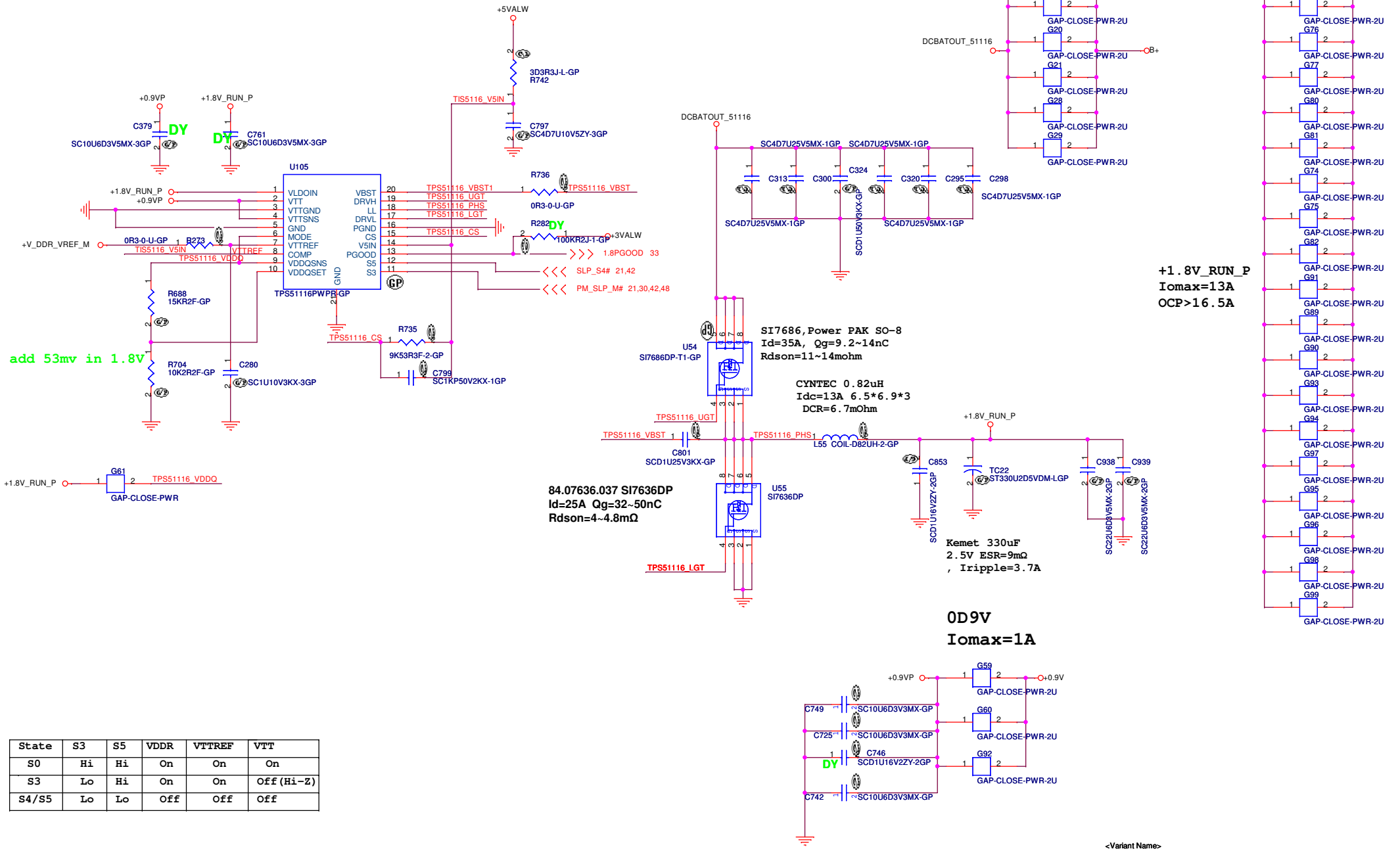
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPA51120 +5VALW +3VALW***

Size: A3 | Document Number: **KARIA - DISCRETE** | Rev: SH

Date: Tuesday, May 20, 2008 | Sheet 46 of 58

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

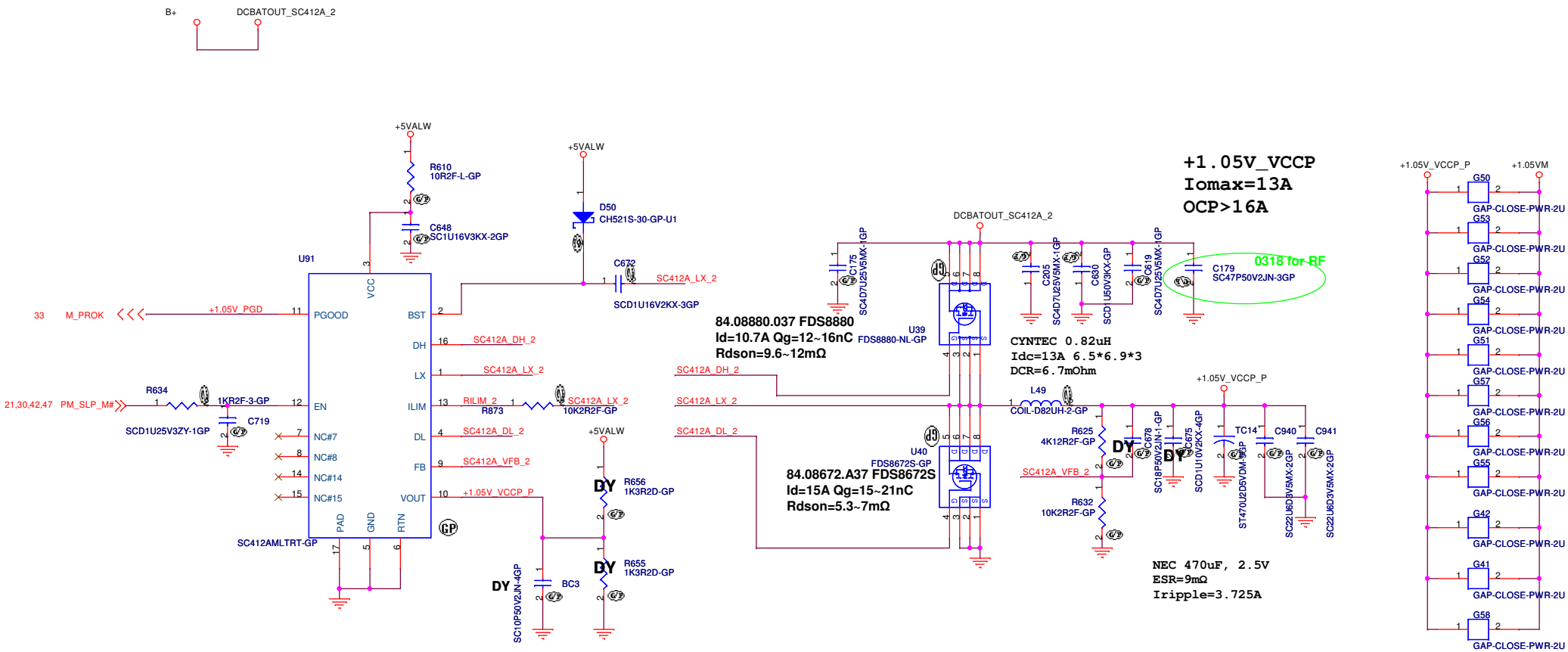
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51116 1D8V/0D9V**

Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

Date: Friday, May 16, 2008 Sheet 47 of 58



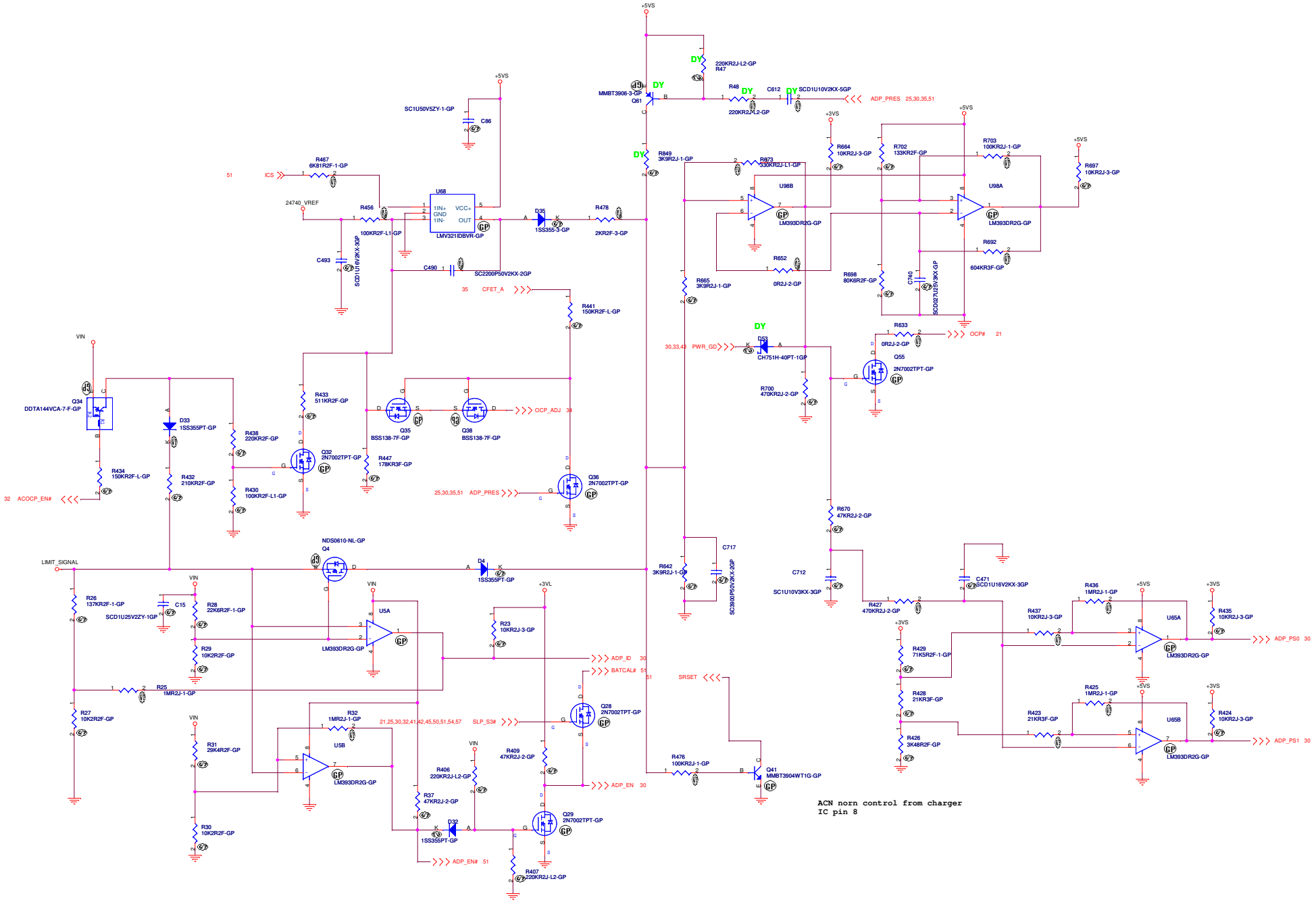
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SC412A +1.05VM

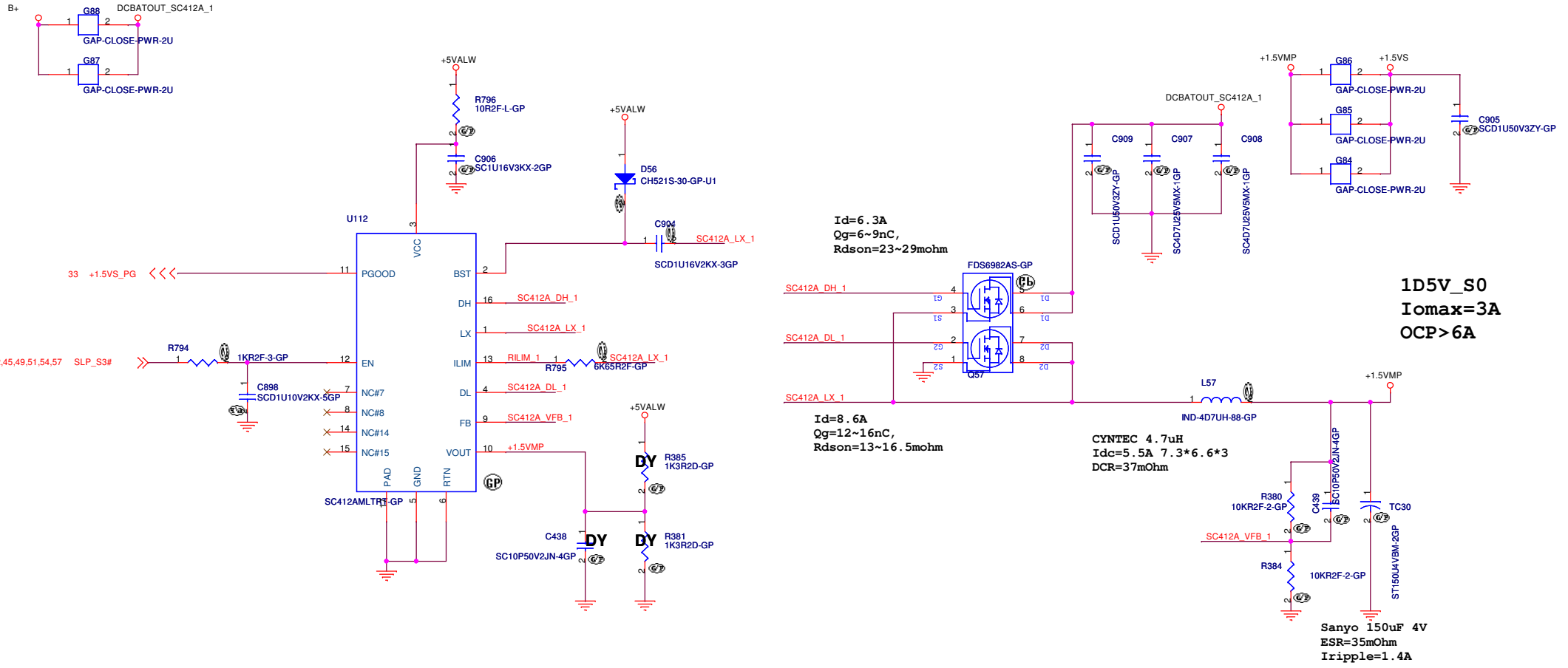
Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

Date: Friday, May 16, 2008 Sheet 48 of 58



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **ADP OCP**		
Size: A2	Document Number: **KARIA - DISCRETE**	Rev: **SH**
Date: Friday, May 16, 2008	Sheet 49 of 58	



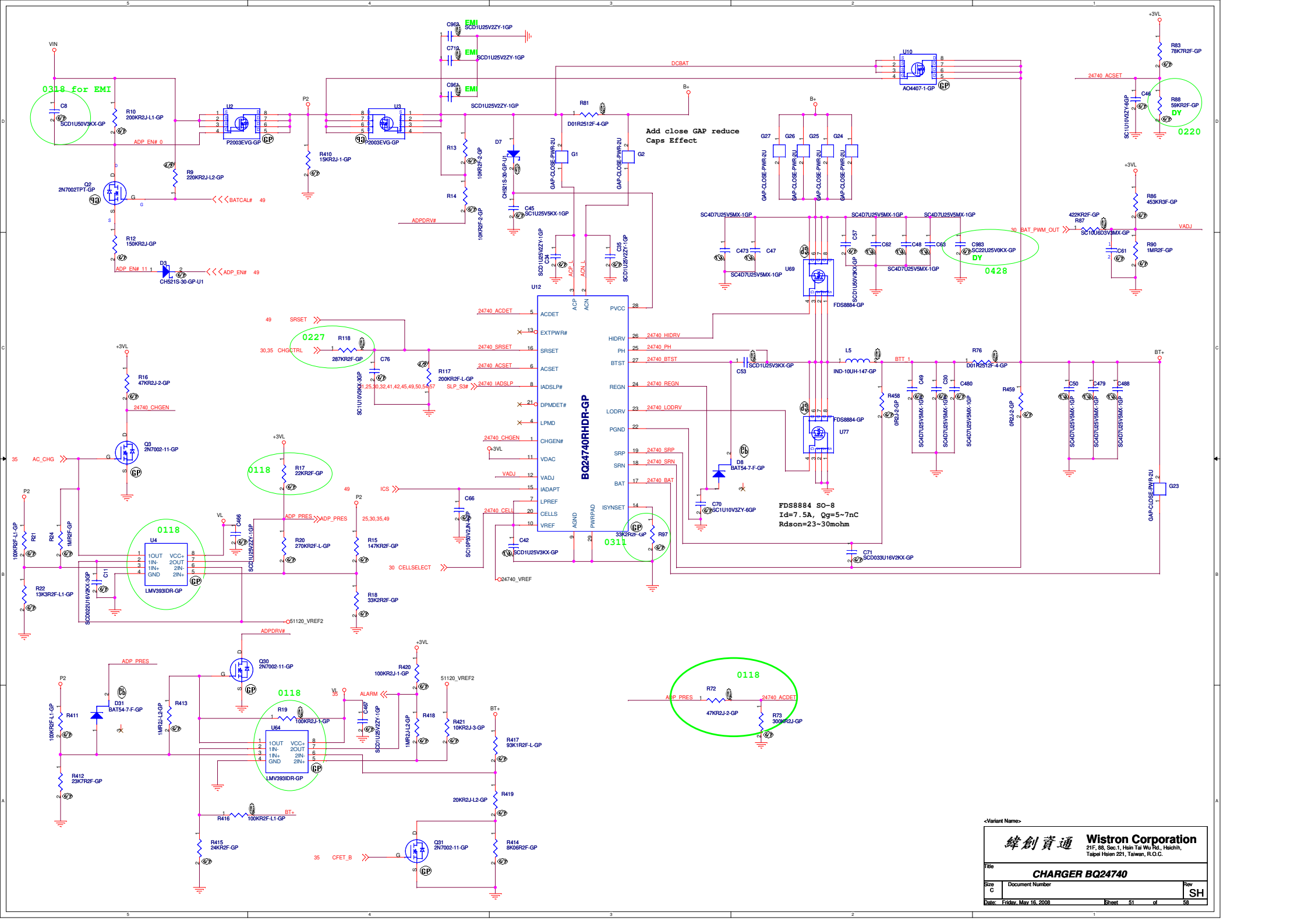
<Variant Name>

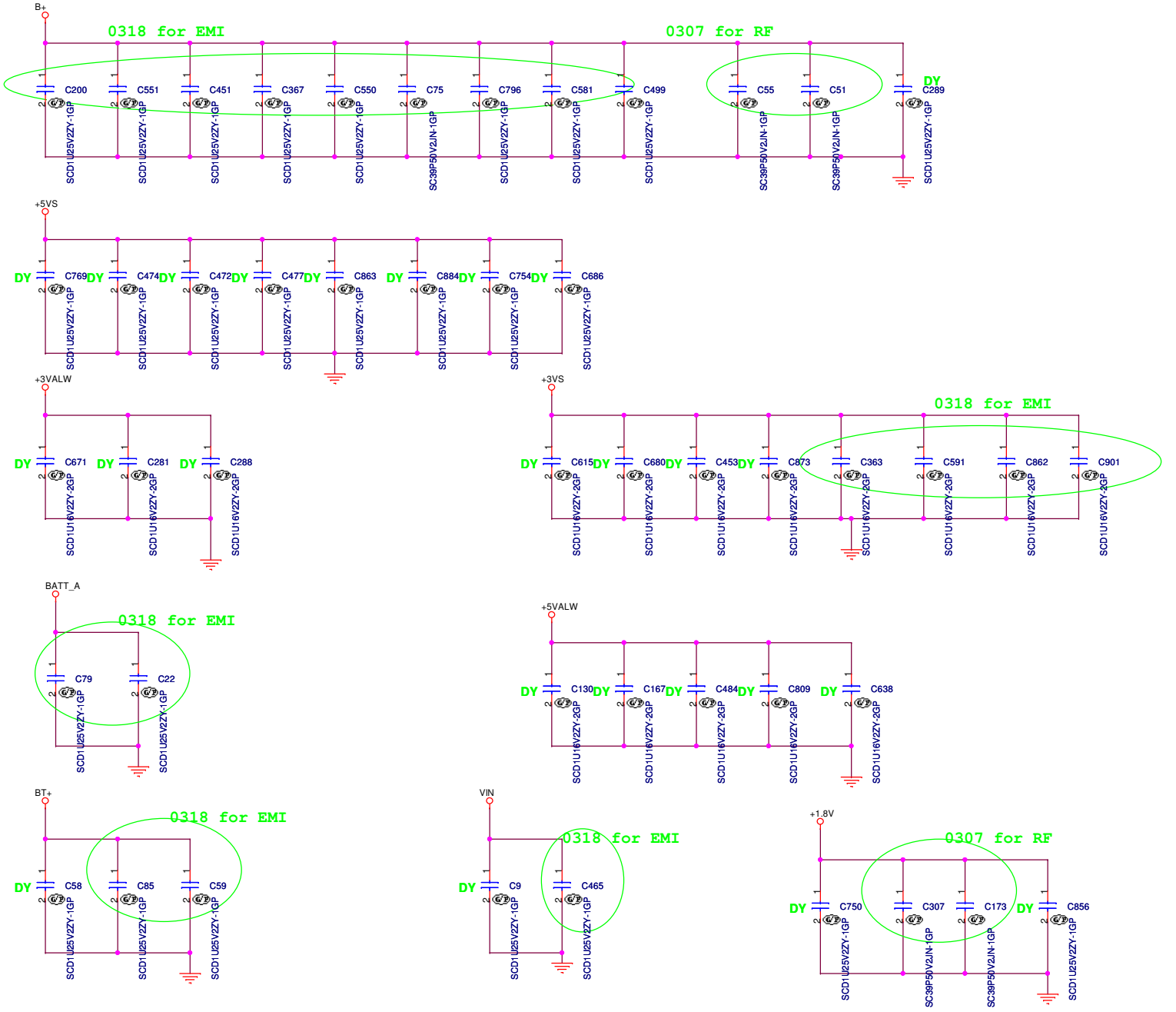
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SC412A_+1.5VS

Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

Date: Friday, May 16, 2008 Sheet 50 of 58


0318 for EMI
Add close GAP reduce Caps Effect
BQ24740RHDR-GP
FDS8884 SO-8
Id=7.5A, Qg=5~7nC
Rdson=23~30mohm
0118
0227
0220
0428
0311
DY
EMI
LMV393IDR-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CHARGER BQ24740
Size C
Document Number
Rev SH
Date: Friday, May 16, 2008
Sheet 51 of 58



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI CAPS***

Size	Document Number	Rev
A3		SH

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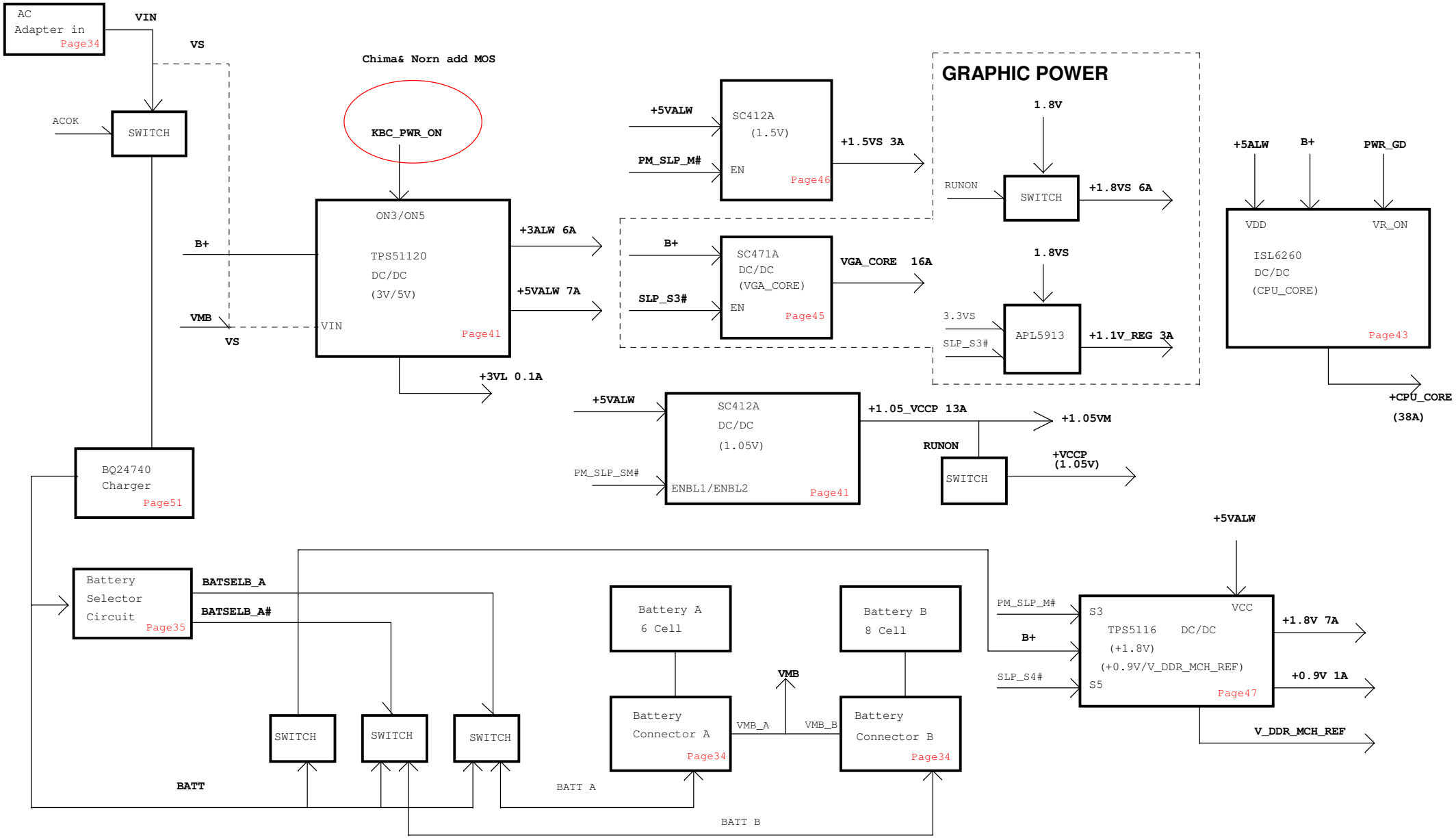


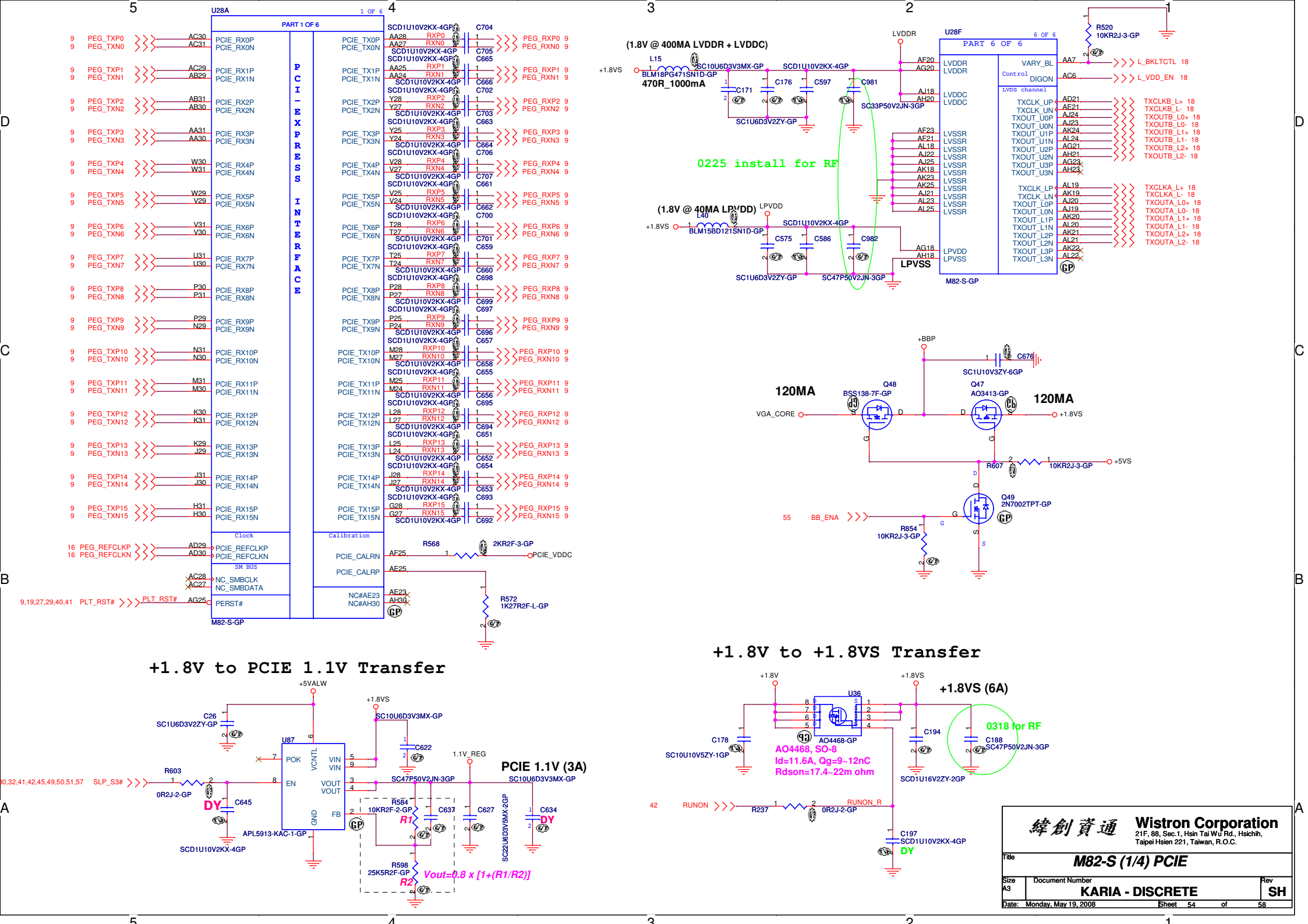
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

Date: Friday, May 16, 2008 Sheet 53 of 58


U28A
PART 1 OF 6
PCI-EXPRESS INTERFACE
PCIE_RX0P
PCIE_RX0N
PCIE_TX0P
PCIE_TX0N
PCIE_RX1P
PCIE_RX1N
PCIE_TX1P
PCIE_TX1N
PCIE_RX2P
PCIE_RX2N
PCIE_TX2P
PCIE_TX2N
PCIE_RX3P
PCIE_RX3N
PCIE_TX3P
PCIE_TX3N
PCIE_RX4P
PCIE_RX4N
PCIE_TX4P
PCIE_TX4N
PCIE_RX5P
PCIE_RX5N
PCIE_TX5P
PCIE_TX5N
PCIE_RX6P
PCIE_RX6N
PCIE_TX6P
PCIE_TX6N
PCIE_RX7P
PCIE_RX7N
PCIE_TX7P
PCIE_TX7N
PCIE_RX8P
PCIE_RX8N
PCIE_TX8P
PCIE_TX8N
PCIE_RX9P
PCIE_RX9N
PCIE_TX9P
PCIE_TX9N
PCIE_RX10P
PCIE_RX10N
PCIE_TX10P
PCIE_TX10N
PCIE_RX11P
PCIE_RX11N
PCIE_TX11P
PCIE_TX11N
PCIE_RX12P
PCIE_RX12N
PCIE_TX12P
PCIE_TX12N
PCIE_RX13P
PCIE_RX13N
PCIE_TX13P
PCIE_TX13N
PCIE_RX14P
PCIE_RX14N
PCIE_TX14P
PCIE_TX14N
PCIE_RX15P
PCIE_RX15N
PCIE_TX15P
PCIE_TX15N
Clock
PCIE_REFCLKP
PCIE_REFCLKN
SM BUS
NC_SMBCLK
NC_SMBDATA
PERST#
Calibration
PCIE_CALRN
PCIE_CALRP
NC#AE23
NC#AH30
M82-S-GP
R568 2KR2F-3-GP
R572 1K27R2F-L-GP
PCIE_VDDC
PLT_RST#
+1.8V to PCIE 1.1V Transfer
+5VALW
+1.8VS
SC10U6D3V3MX-GP
C26
SC1U6D3V2ZY-GP
U87
APL5913-KAC-1-GP
POK
EN
VCNTL
VIN
VOUT
GND
FB
R603
0R2J-2-GP
DY
C645
SCD1U10V2KX-4GP
C622
SC47P50V2JN-3GP
1.1V_REG
PCIE 1.1V (3A)
SC10U6D3V3MX-GP
R584
10KR2F-2-GP
R1
C637
C627
C634
DY
SC22U6D3V5MX-2GP
R598
25K5R2F-GP
R2
Vout=0.8 x [1+(R1/R2)]
SLP_S3#
+1.8V to +1.8VS Transfer
+1.8V
+1.8VS
U36
AO4468-GP
AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm
C178
SC10U10V5ZY-1GP
C194
SCD1U16V2ZY-2GP
+1.8VS (6A)
0318 for RF
C188
SC47P50V2JN-3GP
RUNON
RUNON_R
R237
0R2J-2-GP
C197
SCD1U10V2KX-4GP
DY
(1.8V @ 400MA LVDDR + LVDDC)
L15
BLM18PG471SN1D-GP
470R_1000mA
C171
C176
C597
C981
SC1U6D3V2ZY-GP
SC33P50V2JN-3GP
LVDDR
U28F
PART 6 OF 6
LVDDR
LVDDC
LVSSR
LPVDD
LPVSS
0225 install for RF
(1.8V @ 40MA LPVDD)
L40
BLM15BD121SN1D-GP
C575
C586
C982
SC47P50V2JN-3GP
R520
10KR2J-3-GP
VARY_BL
DIGON
LVDS channel
L_BKLTCTL
L_VDD_EN
TXCLK_UP
TXCLK_UN
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXCLK_LP
TXCLK_LN
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
M82-S-GP
+BBP
C676
SC1U10V3ZY-6GP
120MA
Q48
BSS138-7F-GP
Q47
AO3413-GP
120MA
VGA_CORE
+1.8VS
R607
10KR2J-3-GP
+5VS
Q49
2N7002TPT-GP
BB_ENA
R854
10KR2J-3-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
M82-S (1/4) PCIE
Size A3
Document Number
KARIA - DISCRETE
Rev SH
Date: Monday, May 19, 2008
Sheet 54 of 58

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

0 = DON'T INSTALL RES
1 = INSTALL 10K RES
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M82-SCE
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M8x)	1
BIF_GEN2_EN_A	GPIO5	ALLOW EITHER PCIE 2.5GT/s OR 5GT/s OPERATION	1
ROM ID CFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X X
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	0
BIF_VGA DIS	PSYNC	VGA ENABLED	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE	1

VRID_[3..0]

GDDR3 64bit 0 0 0 0 / 0 1 0 1 / 1 0

00 -->8M*32
01 -->16M*32
10 -->32M*32

00 -->Qimonda
01 -->Samsung

VRAM Configuration	Install Resistors	
Samsung 16x32MB	R134, R125, R119, R114	<-- Default
Samsung 32x32MB	R131, R121, R119, R114	
Qimonda 16x32MB	R134, R125, R119, R113	
Qimonda 32x32MB	R131, R121, R119, R113	

VRAM ID

Aperture Config PIN	M82SCE GPIO	Strapping Resistor	64MB VRAM	128MB VRAM	256MB VRAM
CONFIG 0	GPIO_11	R597	0	0	1
CONFIG 1	GPIO_12	R831	1	0	0
CONFIG 2	GPIO_13	R832	0	0	0
CONFIG 3	GPIO_9	TP88	X	X	X

U28B PART 2 OF 6 (2 OF 6)

INTEGRATED TMDS/DP PORT
EXT TMDS DVO
DAC1 / CRT
DAC2 (TV/CRT2)
GENERAL PURPOSE I/O
SERIAL BUSES
PLL & XTAL
THERMAL
TEST

PLACE THESE CAPACITOR CLOSE TO CONNECTOR

PLACE THESE RESISTORS CLOSE TO DIFF. PAIRS AND AVOID STUBS TO ALL DIFF. TRACES.

MINIMIZE THE DISTANCE BETWEEN THESE RES. AND 100nF AC CAPS

Route RB, GB and BB as differential complement of R, G, and B signals to VGA connector and docking connector

Un-install to disable HD-Audio function

(1.8V @ 40MA DPLL_PVDD)
(1.8V @ 40MA PCIE_PVDD)
120 OHM 450MA
(.95V-1.1V @ 230MA MPVDD)
(DPLL_VDDC 1.1V @ 100 MA)

VREFG = VDDR4.5(1.8V) / 3=0.6V
PLACE VREF DIVIDER AND CAP CLOSE TO ASIC

VOLTAGE DIVIDER TO MAKE XTALIN VOLTAGE LEVEL OF 1.8V

PULLUP POWER RAIL MUST BE UP BEFORE CORE POWER RAIL

(1.1V @ 400MA TPVDD)
(1.8V @ 20MA TPVDD FACH)
(1.8V @ 65MA AVDD)
(1.8V @ 100MA VDD1DI,VDD2DI)
(3.3V @ 135MA A2VDD)
(1.8V @ 2MA A2VDDQ)

3.3V TO 5V LEVEL SHIFT LOGIC REQUIRED:
M82-S: DDC1 & 2 (DDC3 & 4 ARE 5V TOLERATNCE)

CRT
ICH
DVI
LVDS

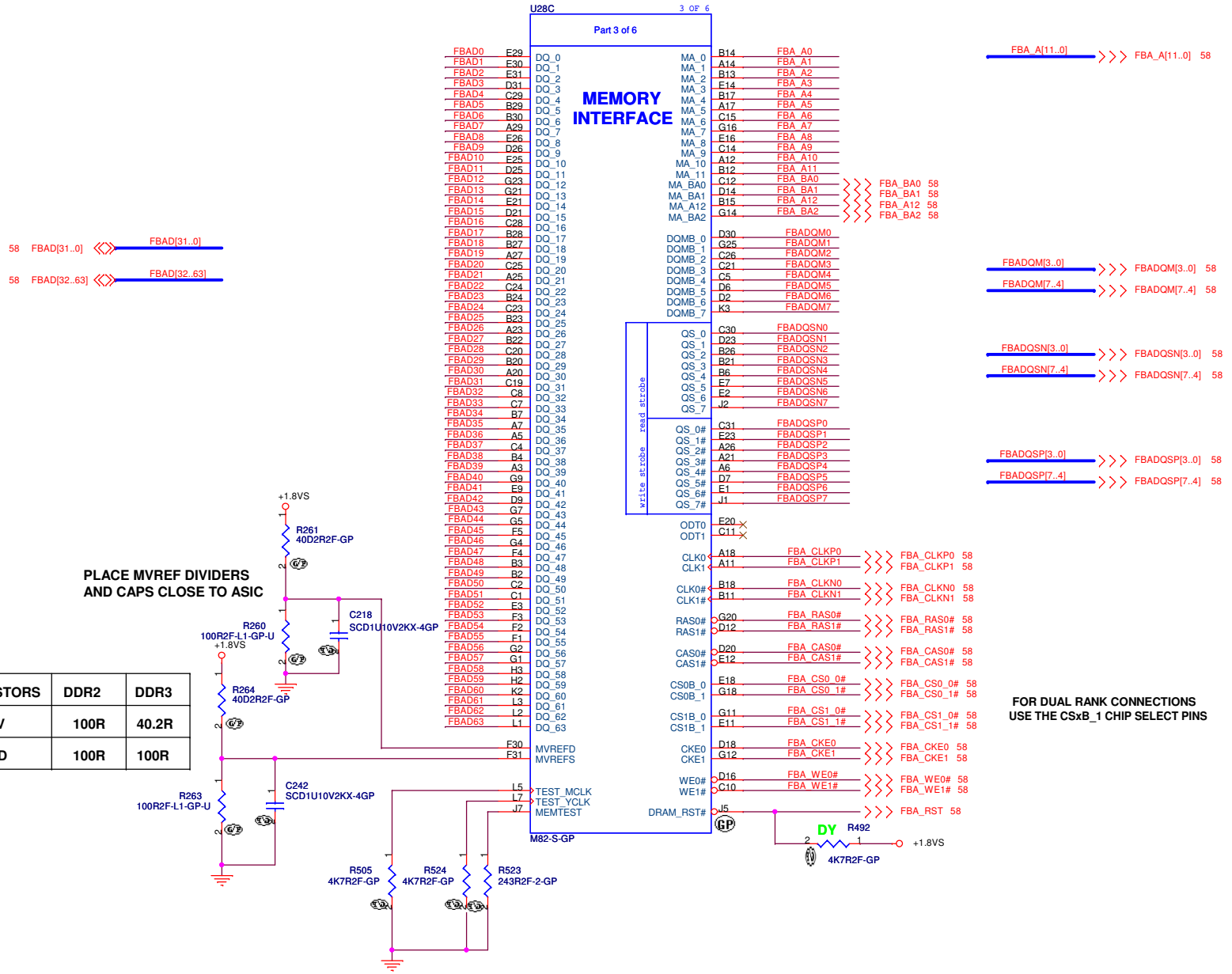
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M82-S (2/4) I/O

Size: Custom | Document Number: KARIA - DISCRETE | Rev: SH

Date: Monday, May 19, 2008 | Sheet 55 of 58



DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

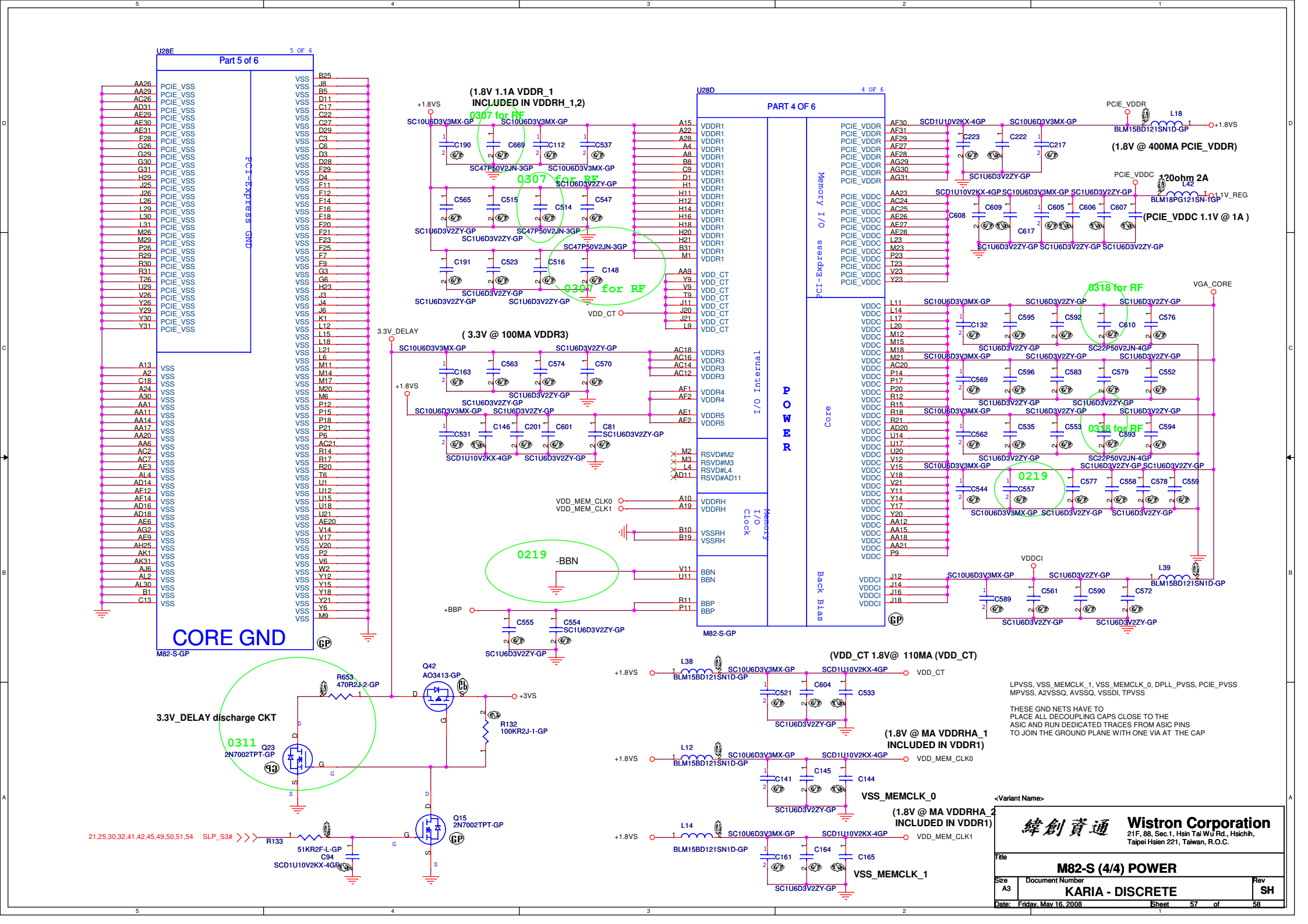
<Variant Name>

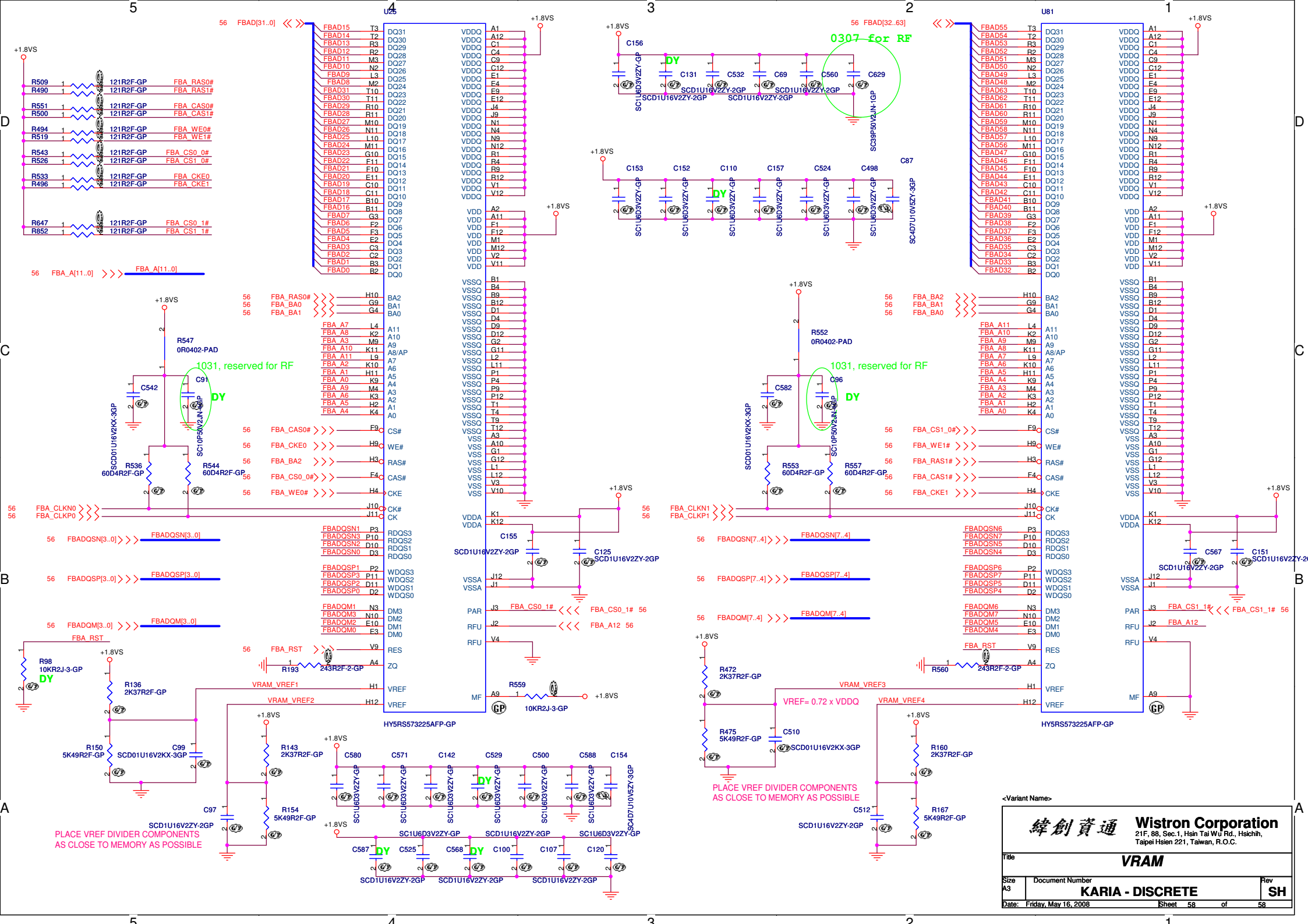
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M82-S (3/4) VRAM Interface

Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

Date: Friday, May 16, 2008 | Sheet 56 of 58


U28E
Part 5 of 6
5 OF 6
PCI-Express GND
PCIE_VSS
VSS
CORE GND
M82-S-GP
U28D
PART 4 OF 6
4 OF 6
POWER
Memory I/O
PCI-Express
I/O Internal
Core
Back Bias
Memory I/O Clock
(1.8V 1.1A VDDR_1
INCLUDED IN VDDRH_1,2)
0307 for RF
(3.3V @ 100MA VDDR3)
3.3V_DELAY
0307 for RF
0307 for RF
0307 for RF
(1.8V @ 400MA PCIE_VDDR)
120ohm 2A
(PCIE_VDDC 1.1V @ 1A)
VGA_CORE
0318 for RF
0318 for RF
0219
0219
-BBN
(VDD_CT 1.8V@ 110MA (VDD_CT)
(1.8V @ MA VDDRHA_1
INCLUDED IN VDDR1)
VSS_MEMCLK_0
(1.8V @ MA VDDRHA_2
INCLUDED IN VDDR1)
VSS_MEMCLK_1
3.3V_DELAY discharge CKT
0311
LPVSS, VSS_MEMCLK_1, VSS_MEMCLK_0, DPLL_PVSS, PCIE_PVSS
MPVSS, A2VSSQ, AVSSQ, VSSDI, TPVSS
THESE GND NETS HAVE TO
PLACE ALL DECOUPLING CAPS CLOSE TO THE
ASIC AND RUN DEDICATED TRACES FROM ASIC PINS
TO JOIN THE GROUND PLANE WITH ONE VIA AT THE CAP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
M82-S (4/4) POWER
Size A3
Document Number
KARIA - DISCRETE
Rev SH
Date: Friday, May 16, 2008
Sheet 57 of 58


U25
U81
HY5RS573225AFP-GP
0307 for RF
1031, reserved for RF
1031, reserved for RF
DY
PLACE VREF DIVIDER COMPONENTS AS CLOSE TO MEMORY AS POSSIBLE
PLACE VREF DIVIDER COMPONENTS AS CLOSE TO MEMORY AS POSSIBLE
VREF= 0.72 x VDDQ
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM
Size A3
Document Number
KARIA - DISCRETE
Rev SH
Date: Friday, May 16, 2008
Sheet 58 of 58