

Compal confidential

Schematics Document

Mobile Merom uFCPGA with Satna Rosa Platform

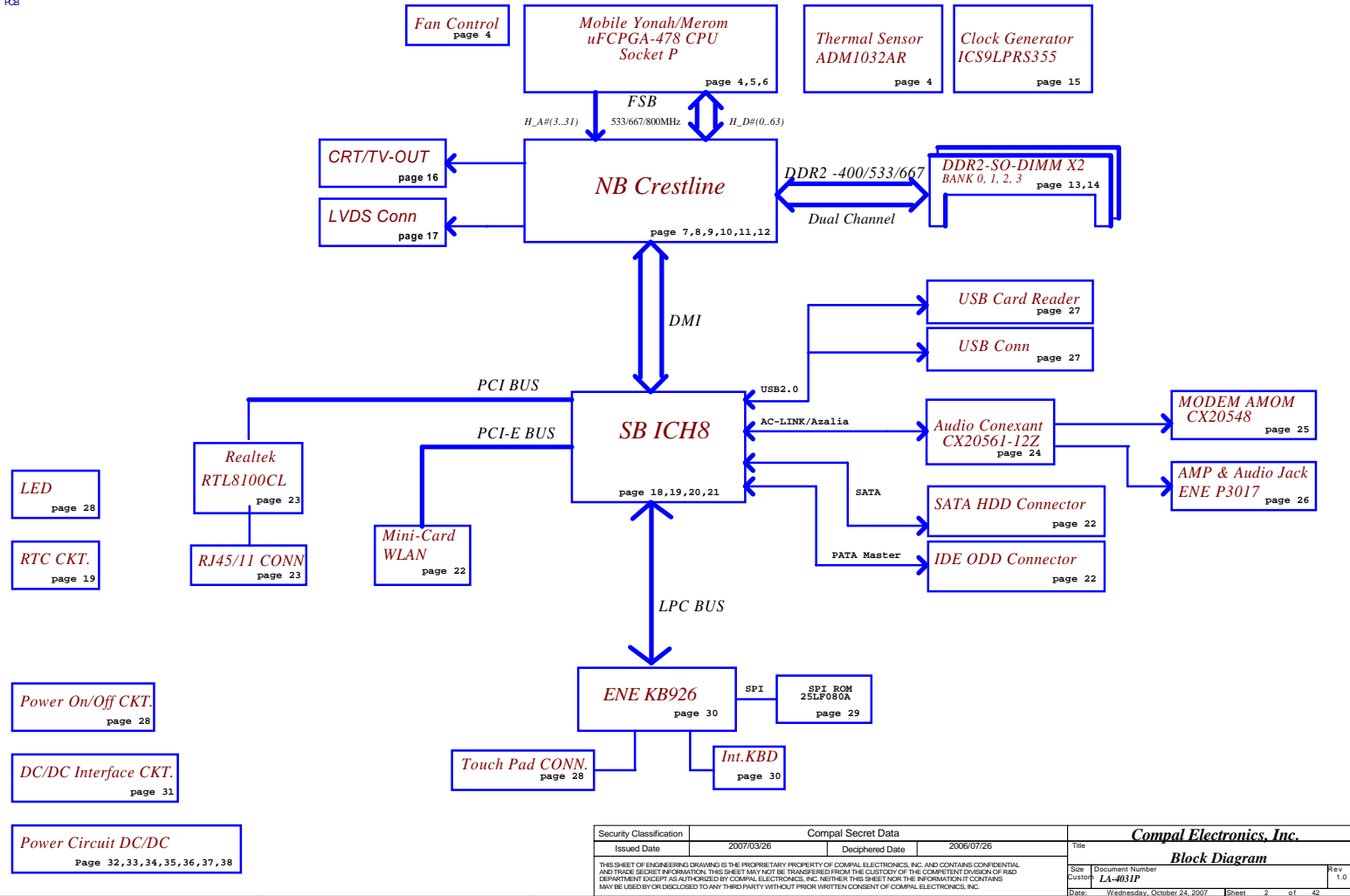
2007-07-30

REV: 0.2

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Spartan 1.1 (Merom +Crestline+ICH8)

ZZZ
PCB



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Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD17	0	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

SMBUS Control Table

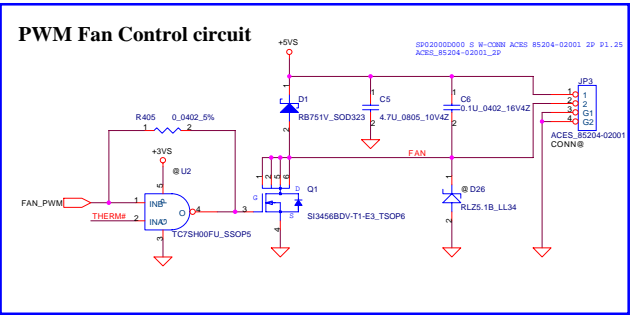
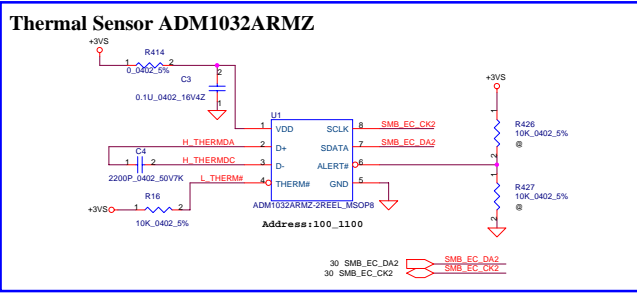
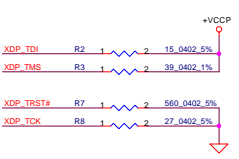
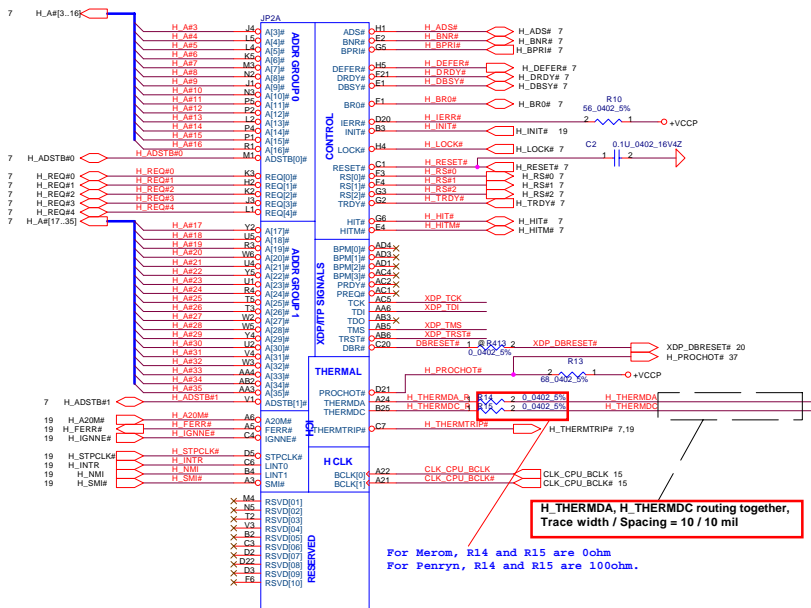
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1022	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CR_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43152432L03(965GM) & 43152432L04(960GML) with card reader

BOM: 43152432L01(965GM) & 43152432L02(960GML) without card reader

Jump-Short: PJP?

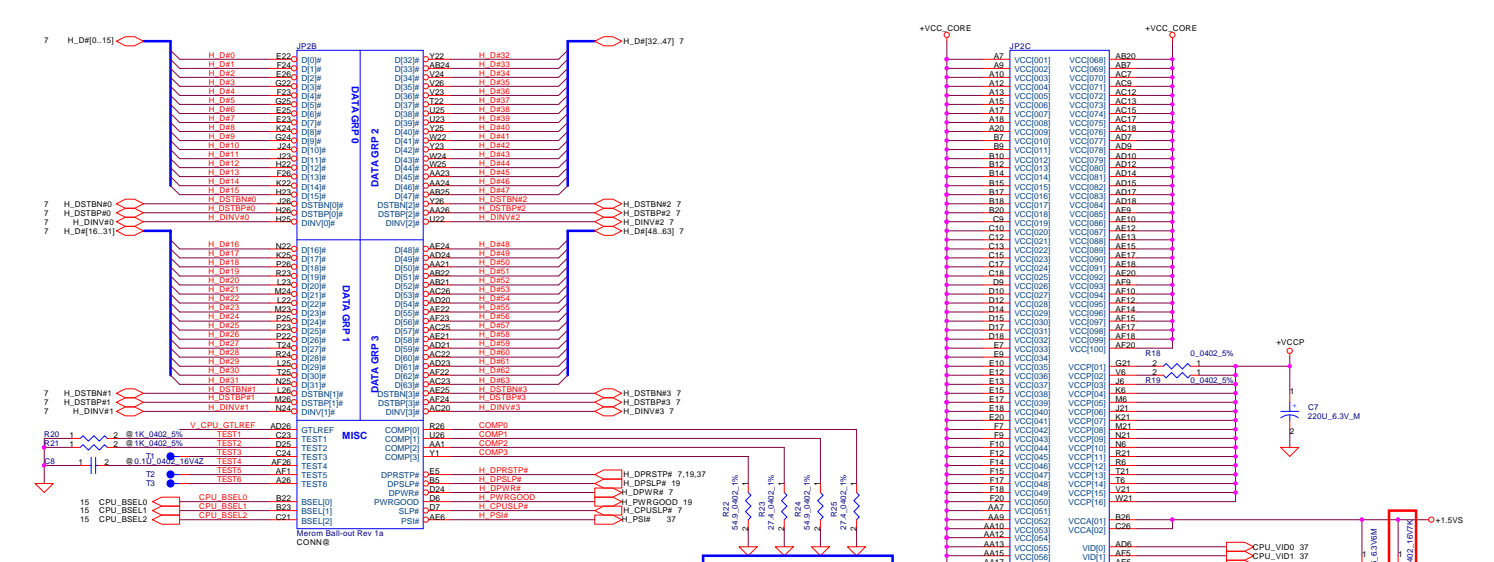
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**H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil**

For Merom, R14 and R15 are 0ohm
For Penryn, R14 and R15 are 100ohm.

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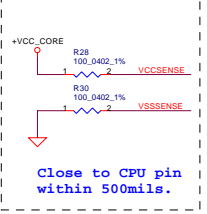
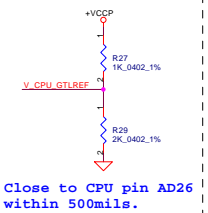


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

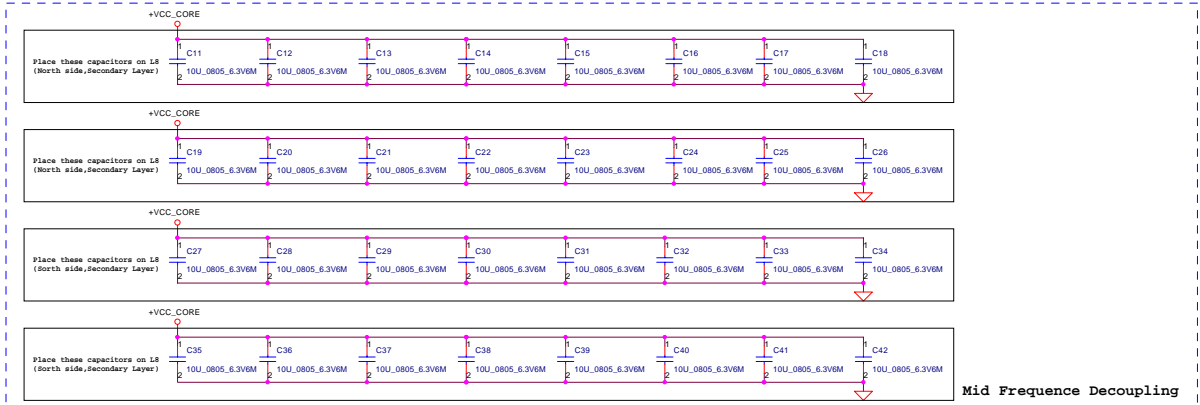
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.
 COMP[0, 2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.



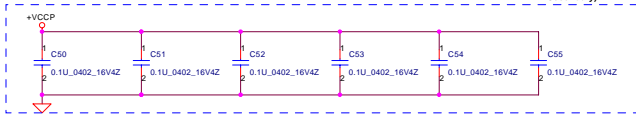
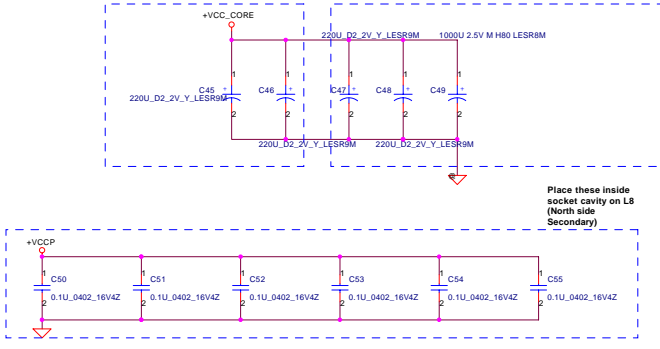
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Compal Electronics, Inc. Merom(2/3)-AGTL+/PWR Size: LA-403P Customer: LA-403P Date: Wednesday, October 24, 2007		Title: Merom(2/3)-AGTL+/PWR Rev: 1.0 Sheet: 5 of 42	

JP2D			
A4	VSS1001	VSS1080	P6
A5	VSS1002	VSS1083	P21
A6	VSS1003	VSS1084	P22
A14	VSS1004	VSS1085	R2
A16	VSS1005	VSS1086	R22
A19	VSS1006	VSS1087	R22
A22	VSS1007	VSS1088	T1
AF2	VSS1008	VSS1089	T1
BB	VSS1009	VSS1090	T4
BB	VSS1010	VSS1091	T7
B11	VSS1011	VSS1092	T26
B13	VSS1012	VSS1093	T17
B18	VSS1013	VSS1094	U6
B19	VSS1014	VSS1095	U2
B21	VSS1015	VSS1096	U24
C2	VSS1016	VSS1097	U5
C2	VSS1017	VSS1098	U2
C3	VSS1018	VSS1099	U22
C4	VSS1019	VSS1100	U25
C14	VSS1020	VSS1101	W1
C19	VSS1021	VSS1102	W4
C16	VSS1022	VSS1103	W22
C2	VSS1023	VSS1104	W2
C22	VSS1024	VSS1105	X3
C2	VSS1025	VSS1106	X6
D1	VSS1026	VSS1107	X2
D4	VSS1027	VSS1108	Y24
D8	VSS1028	VSS1109	Y2
D11	VSS1029	VSS1110	Y24
D13	VSS1030	VSS1111	Y8
D18	VSS1031	VSS1112	AA1
D19	VSS1032	VSS1113	AA4
D23	VSS1033	VSS1114	AA16
D28	VSS1034	VSS1115	AA19
E3	VSS1035	VSS1116	AA2
E8	VSS1036	VSS1117	AA25
E8	VSS1037	VSS1118	AB1
E11	VSS1038	VSS1119	AB4
E14	VSS1039	VSS1120	AB6
E16	VSS1040	VSS1121	AB11
E19	VSS1041	VSS1122	AB13
E21	VSS1042	VSS1123	AB16
E24	VSS1043	VSS1124	AB19
F4	VSS1044	VSS1125	AB23
F8	VSS1045	VSS1126	AB26
F11	VSS1046	VSS1127	AC2
F18	VSS1047	VSS1128	AC6
F19	VSS1048	VSS1129	AC11
F21	VSS1049	VSS1130	AC14
F2	VSS1050	VSS1131	AC16
F22	VSS1051	VSS1132	AC19
F25	VSS1052	VSS1133	AC21
G4	VSS1053	VSS1134	AC24
G3	VSS1054	VSS1135	AD2
G28	VSS1055	VSS1136	AD5
H8	VSS1056	VSS1137	AD8
H8	VSS1057	VSS1138	AD11
H21	VSS1058	VSS1139	AD13
H24	VSS1059	VSS1140	AD16
J2	VSS1060	VSS1141	AD19
J2	VSS1061	VSS1142	AD22
J22	VSS1062	VSS1143	AD25
K5	VSS1063	VSS1144	AE1
K1	VSS1064	VSS1145	AE4
K1	VSS1065	VSS1146	AE8
K4	VSS1066	VSS1147	AE11
K29	VSS1067	VSS1148	AE16
K28	VSS1068	VSS1149	AE14
L3	VSS1069	VSS1150	AE16
L6	VSS1070	VSS1151	AE19
L1	VSS1071	VSS1152	AE23
L24	VSS1072	VSS1153	AE26
M2	VSS1073	VSS1154	AF
M2	VSS1074	VSS1155	AF
M22	VSS1075	VSS1156	AF8
M28	VSS1076	VSS1157	AF11
N1	VSS1077	VSS1158	AF13
N4	VSS1078	VSS1159	AF16
N23	VSS1079	VSS1160	AF19
N28	VSS1080	VSS1161	AF21
P1	VSS1081	VSS1162	AZ2
		VSS1163	AZ5

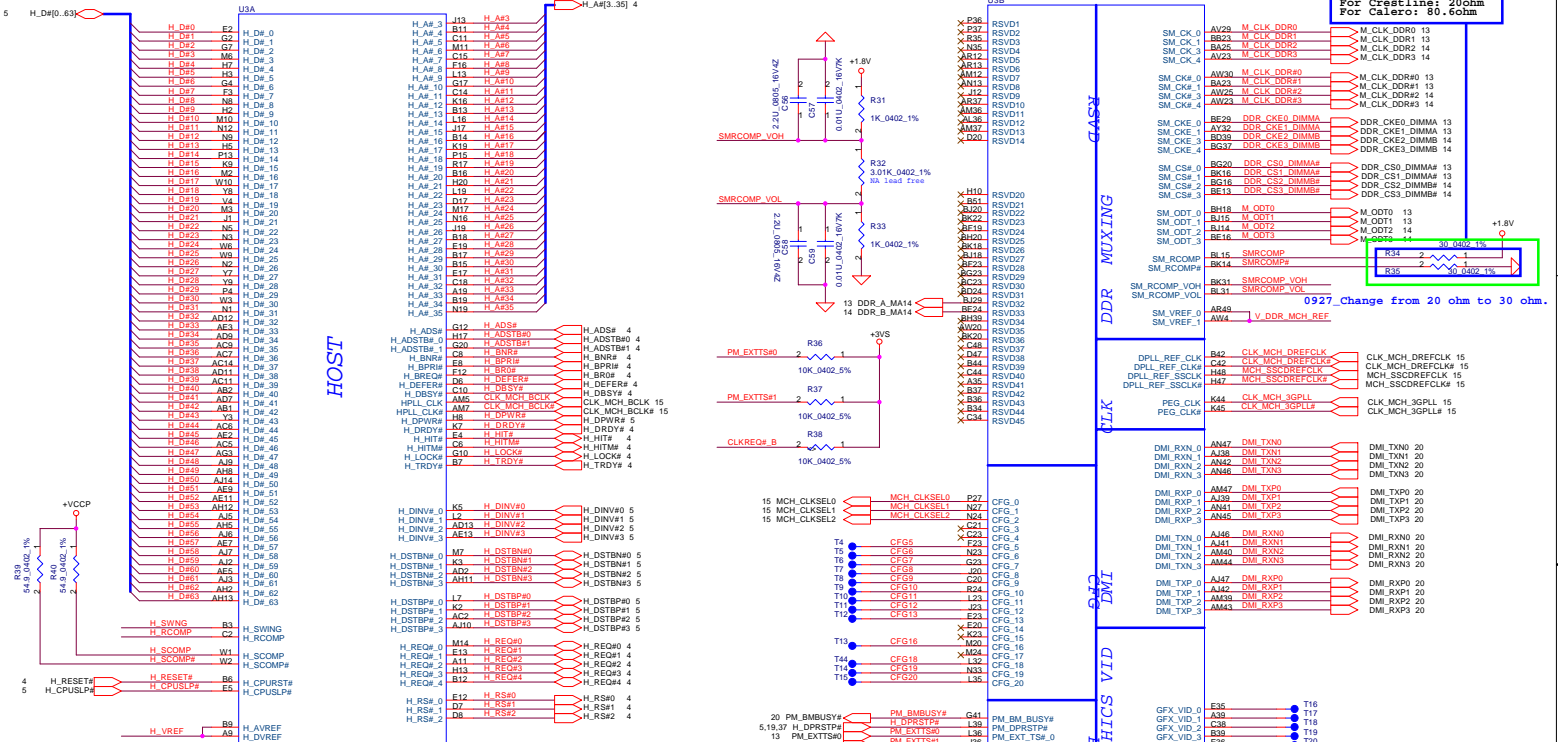


Mid Frequency Decoupling

Near CPU CORE regulator ESR <= 1.5m ohm Capacitor > 1980uF



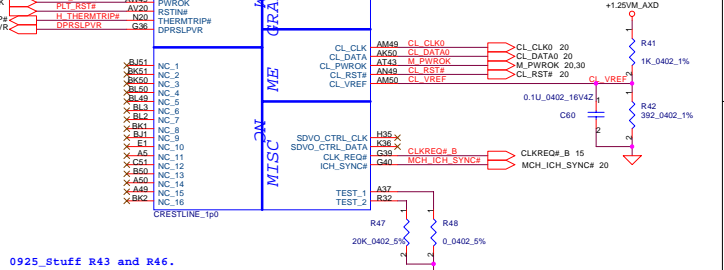
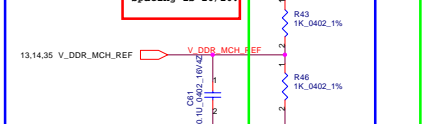
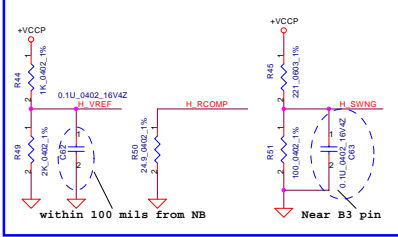
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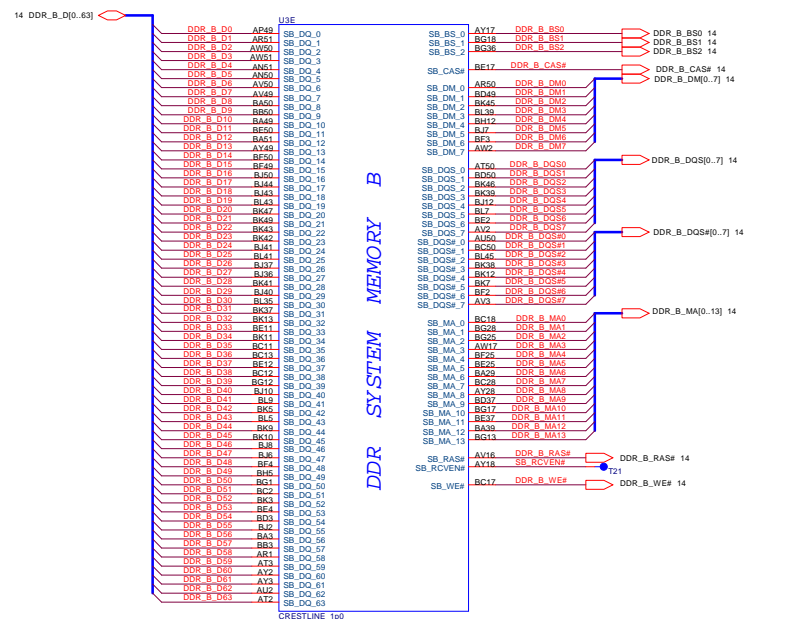
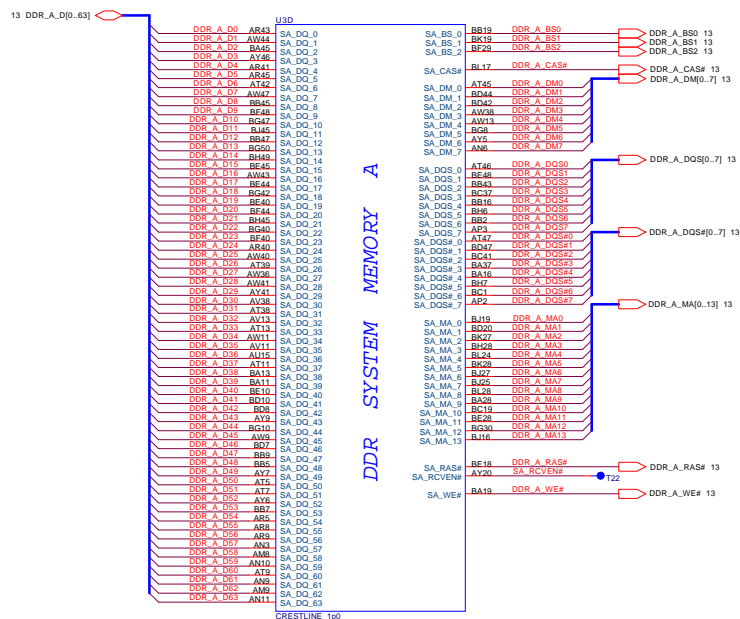
layout note:
Route H_SCOMP and H_SCMP# with trace width, spacing and impedance (55 ohm) same as F8B data traces

Layout Note:
H_RCMP / H_VREF / H_SWNG trace width and spacing is 10/20

Layout Note:
V_DDR_MCH_REF trace width and spacing is 20/20.



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CRESTLINE_1p0

CRESTLINE_1p0

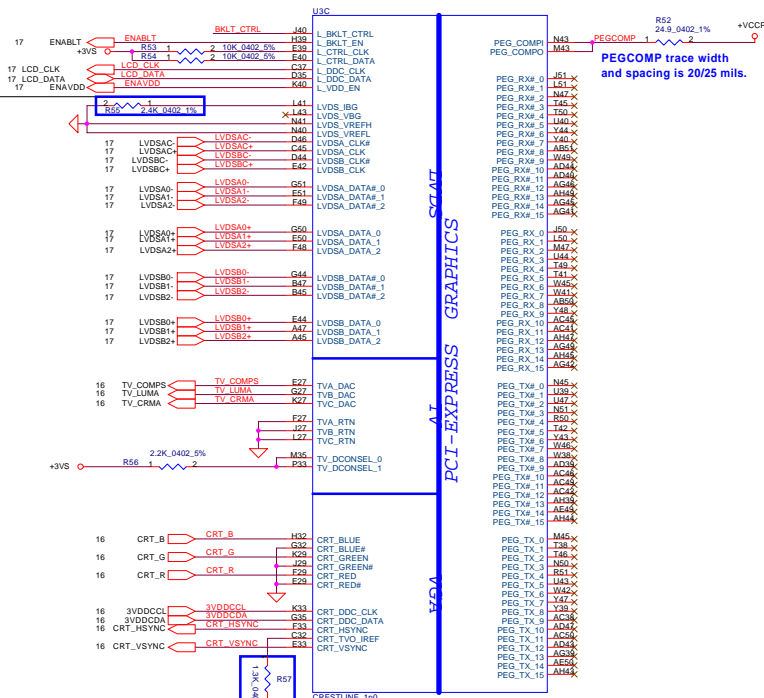
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Issued Date	2007/03/26	Deciphered Date	2006/03/10	CRESTLINE((2/6)-DDR2 A/B CH	
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Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

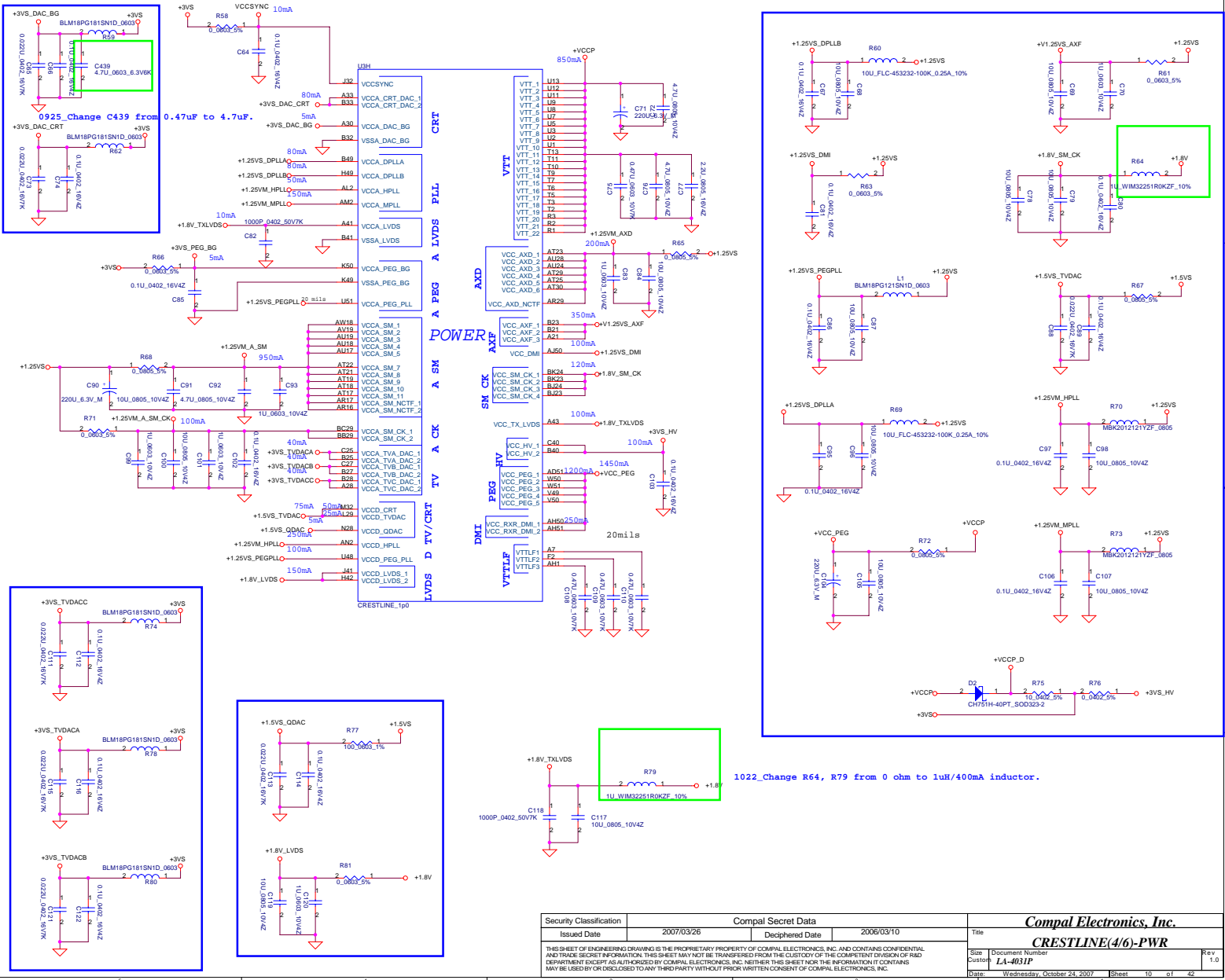
For Crestline: 2.4kohm
For Calero: 1.5kohm



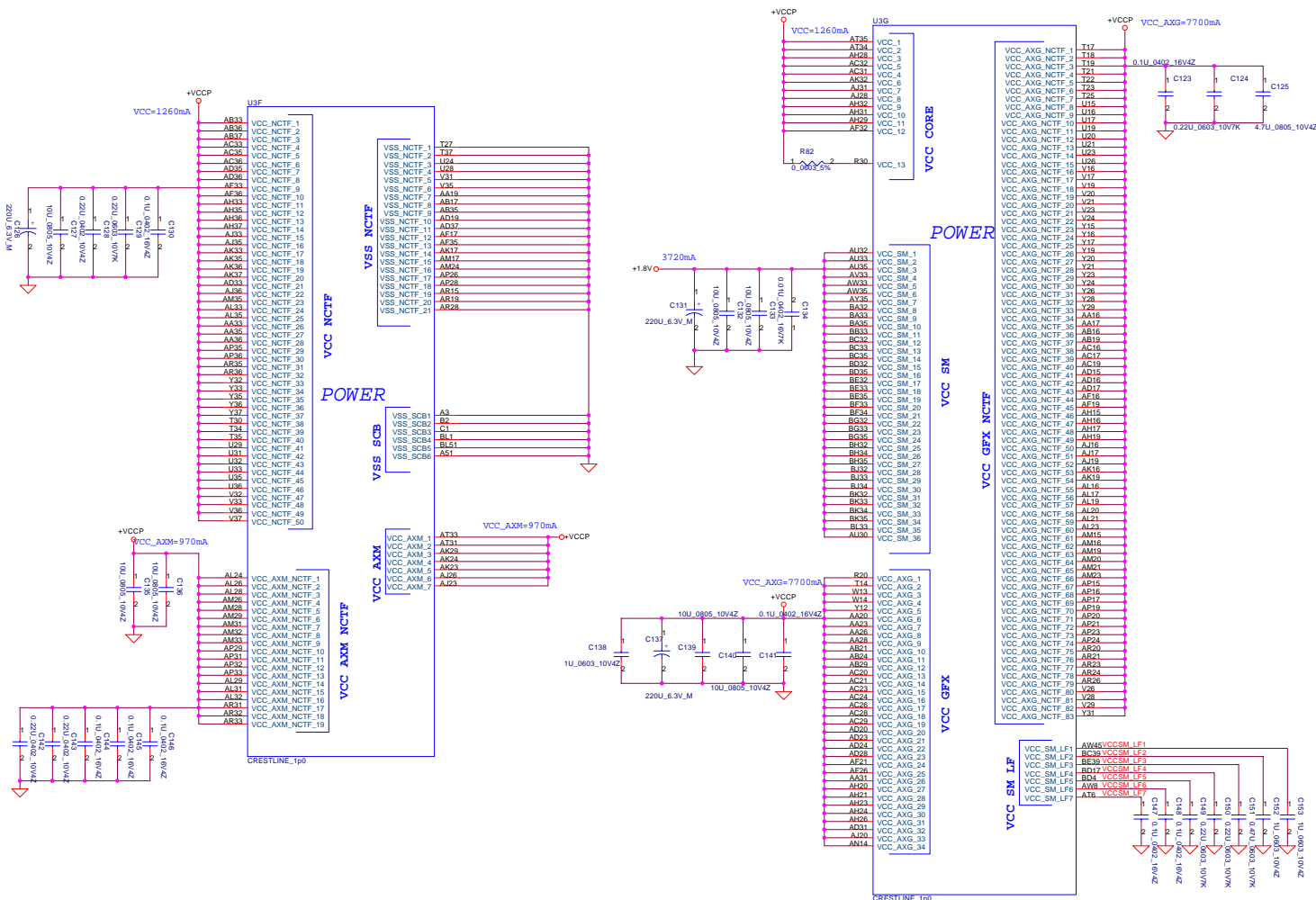
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CRESTLINE(3/6)-VGA/LVDS/TV

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CRESTLINE((5/6)-PWR/GND

U31

A13	VSS_1	AW24
A15	VSS_2	AW23
A17	VSS_3	AW22
A2	VSS_4	AW21
AA21	VSS_5	AW20
AA24	VSS_6	AW19
AA25	VSS_7	AW18
AB20	VSS_8	AW17
AB23	VSS_9	AW16
AB26	VSS_10	AW15
AB28	VSS_11	AW14
AB31	VSS_12	AW13
AC10	VSS_13	AW12
AC13	VSS_14	AW11
AC1	VSS_15	AW10
AC2	VSS_16	AW9
AC43	VSS_17	AW8
AD1	VSS_18	AW7
AD21	VSS_19	AW6
AD26	VSS_20	AW5
AD29	VSS_21	AW4
AD3	VSS_22	AW3
AD41	VSS_23	AW2
AD49	VSS_24	AW1
AD5	VSS_25	AW0
AD5	VSS_26	AW0
AD50	VSS_27	AW0
AE10	VSS_28	AW0
AE14	VSS_29	AW0
AE1	VSS_30	AW0
AE1	VSS_31	AW0
AE1	VSS_32	AW0
AF23	VSS_33	AW0
AF24	VSS_34	AW0
AF24	VSS_35	AW0
AF31	VSS_36	AW0
AG2	VSS_37	AW0
AG38	VSS_38	AW0
AG43	VSS_39	AW0
AG47	VSS_40	AW0
AH3	VSS_41	AW0
AH9	VSS_42	AW0
AH41	VSS_43	AW0
AH9	VSS_44	AW0
AH7	VSS_45	AW0
AI9	VSS_46	AW0
AJ11	VSS_47	AW0
AJ3	VSS_48	AW0
AJ21	VSS_49	AW0
AJ24	VSS_50	AW0
AJ29	VSS_51	AW0
AJ32	VSS_52	AW0
AJ43	VSS_53	AW0
AJ45	VSS_54	AW0
AJ45	VSS_55	AW0
AK20	VSS_56	AW0
AK21	VSS_57	AW0
AK28	VSS_58	AW0
AK28	VSS_59	AW0
AK31	VSS_60	AW0
AK51	VSS_61	AW0
AL1	VSS_62	AW0
AM11	VSS_63	AW0
AM3	VSS_64	AW0
AM4	VSS_65	AW0
AM41	VSS_66	AW0
AN1	VSS_67	AW0
AN45	VSS_68	AW0
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AN43	VSS_72	AW0
AN7	VSS_73	AW0
AN7	VSS_74	AW0
AP4	VSS_75	AW0
AP48	VSS_76	AW0
AP50	VSS_77	AW0
AR1	VSS_78	AW0
AR2	VSS_79	AW0
AR2	VSS_80	AW0
AR44	VSS_81	AW0
AR7	VSS_82	AW0
AT10	VSS_84	AW0
AT14	VSS_85	AW0
AT41	VSS_86	AW0
AT6	VSS_87	AW0
AU1	VSS_88	AW0
AU23	VSS_89	AW0
AU2	VSS_90	AW0
AU36	VSS_91	AW0
AU3	VSS_92	AW0
AU49	VSS_93	AW0
AU4	VSS_94	AW0
AU38	VSS_95	AW0
AV48	VSS_96	AW0
AW1	VSS_97	AW0
AW12	VSS_98	AW0
AW16	VSS_99	AW0

VSS

CRESTLINE_1p0

U31

C46	VSS_199	W11
C50	VSS_200	W39
C7	VSS_201	W43
D13	VSS_202	W47
D24	VSS_203	W5
D3	VSS_204	W7
D32	VSS_205	W13
D39	VSS_206	W2
D45	VSS_207	W41
D49	VSS_208	W46
E10	VSS_209	W49
E14	VSS_210	W5
E24	VSS_211	W50
E28	VSS_212	W51
E32	VSS_213	W52
E47	VSS_214	W59
F19	VSS_215	W61
F36	VSS_216	W62
F4	VSS_217	W63
F40	VSS_218	W64
F50	VSS_219	W65
G1	VSS_220	W66
G13	VSS_221	W67
G16	VSS_222	W68
G19	VSS_223	W69
G24	VSS_224	W70
G28	VSS_225	W71
G28	VSS_226	W72
G34	VSS_227	W73
G42	VSS_228	W74
G46	VSS_229	W75
G48	VSS_230	W76
G4	VSS_231	W77
H24	VSS_232	W78
H28	VSS_233	W79
H4	VSS_234	W80
H45	VSS_235	W81
J11	VSS_236	W82
J16	VSS_237	W83
J2	VSS_238	W84
J24	VSS_239	W85
J33	VSS_240	W86
J36	VSS_241	W87
J39	VSS_242	W88
J43	VSS_243	W89
K12	VSS_245	W90
K47	VSS_246	W91
L1	VSS_247	W92
L17	VSS_248	W93
L20	VSS_249	W94
L24	VSS_250	W95
L28	VSS_251	W96
L3	VSS_252	W97
L33	VSS_253	W98
L48	VSS_254	W99
M28	VSS_255	W100
M42	VSS_256	W101
M45	VSS_257	W102
M46	VSS_258	W103
M49	VSS_259	W104
M5	VSS_260	W105
M50	VSS_261	W106
M9	VSS_262	W107
N14	VSS_263	W108
N17	VSS_264	W109
N29	VSS_265	W110
N32	VSS_266	W111
N33	VSS_267	W112
N39	VSS_268	W113
N44	VSS_269	W114
N49	VSS_270	W115
N7	VSS_271	W116
P13	VSS_272	W117
P2	VSS_273	W118
P23	VSS_274	W119
P2	VSS_275	W120
P3	VSS_276	W121
P39	VSS_277	W122
R49	VSS_278	W123
T39	VSS_279	W124
T43	VSS_280	W125
T47	VSS_281	W126
T47	VSS_282	W127
U41	VSS_283	W128
U50	VSS_284	W129
V2	VSS_285	W130
V3	VSS_286	W131

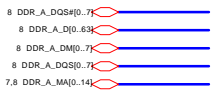
VSS

CRESTLINE_1p0

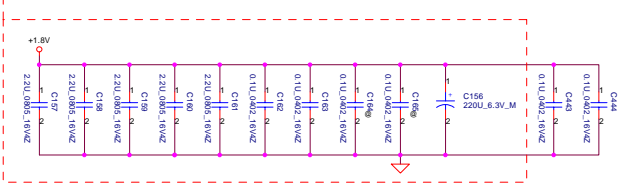
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Issued Date	2007/03/26	Deciphered Date	2006/03/10	Customer
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Date: Wednesday, October 24, 2007				Sheet 12 of 42

Compal Electronics, Inc.
CRESTLINE((6/6)-PWR/GND

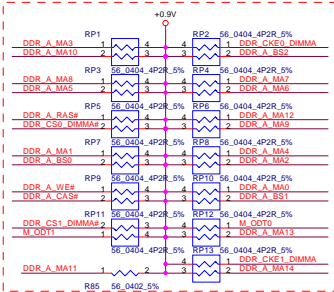
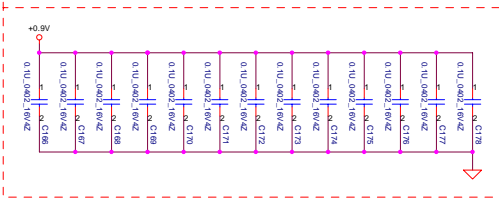
Customer: LA-4031P



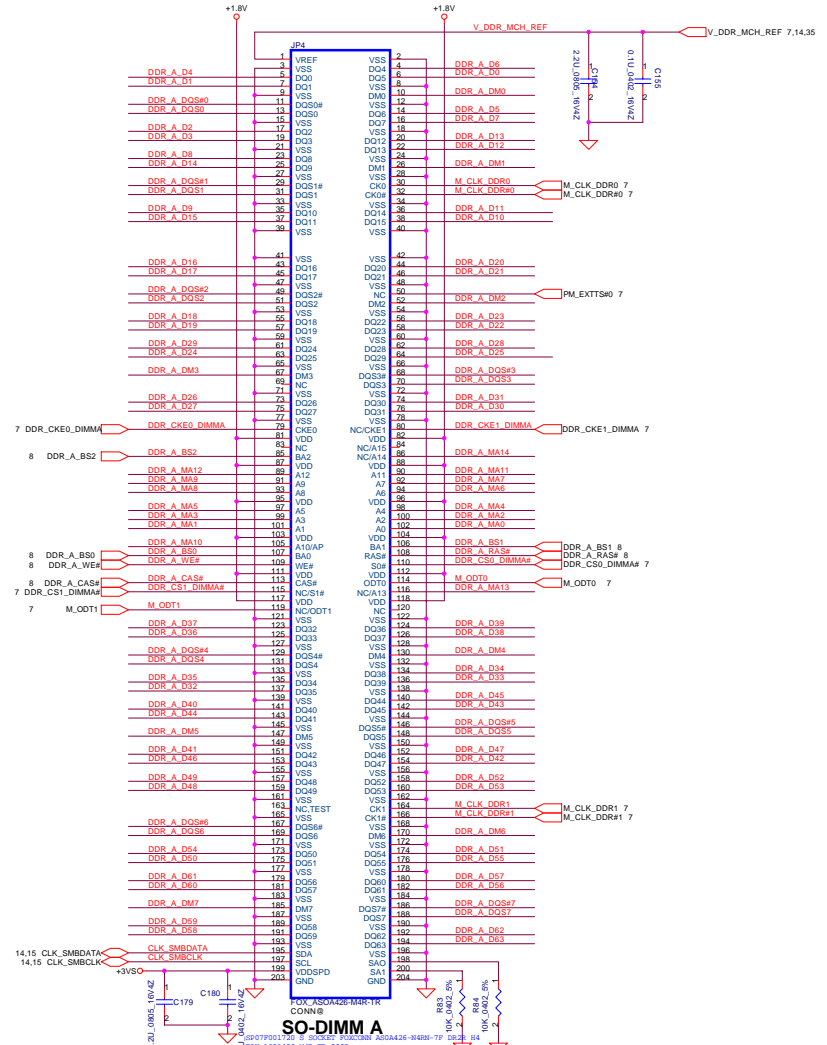
Layout Note:
Place near JP34



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



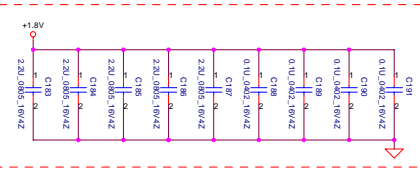
Layout Note:
Place these resistor
closely JP34, all
trace length Max=1.5"



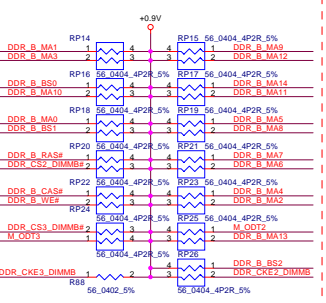
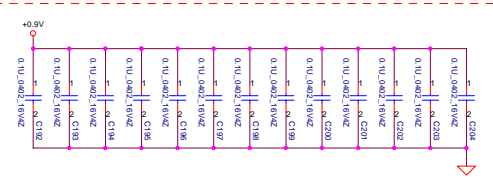
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Issued Date	2007/03/26	Deciphered Date	2006/03/10
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</p>			
<p style="text-align: right;">Compal Electronics, Inc. DDR2-SODIMM SLOT1</p>			<p>Title</p>
<p>Size: Document Number Customer: LA-401P</p>			<p>Rev: 1.0</p>
<p>Date: Wednesday, October 24, 2007</p>			<p>Sheet: 13 of 42</p>

- 8 DDR_B_DQS#(0..7)
- 8 DDR_B_DQ(0..63)
- 8 DDR_B_DM(0..7)
- 8 DDR_B_DQS(0..7)
- 7.8 DDR_B_MA(0..14)

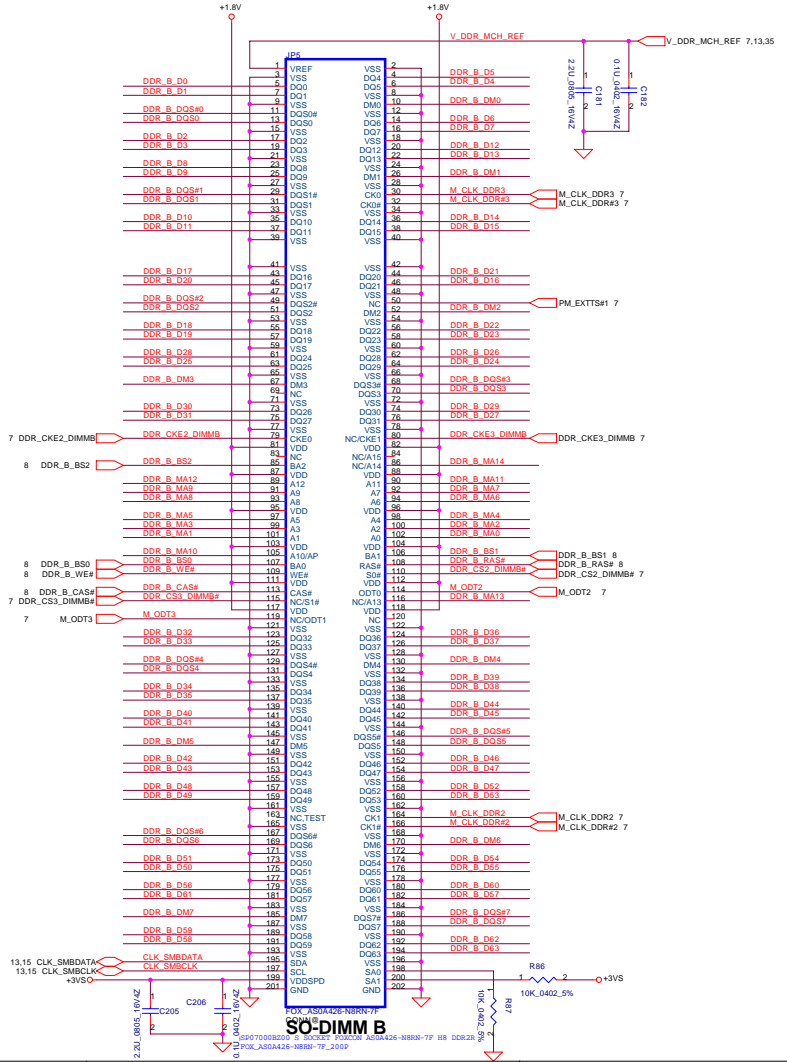
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place these resistor closely JP10, all trace length Max=1.5"



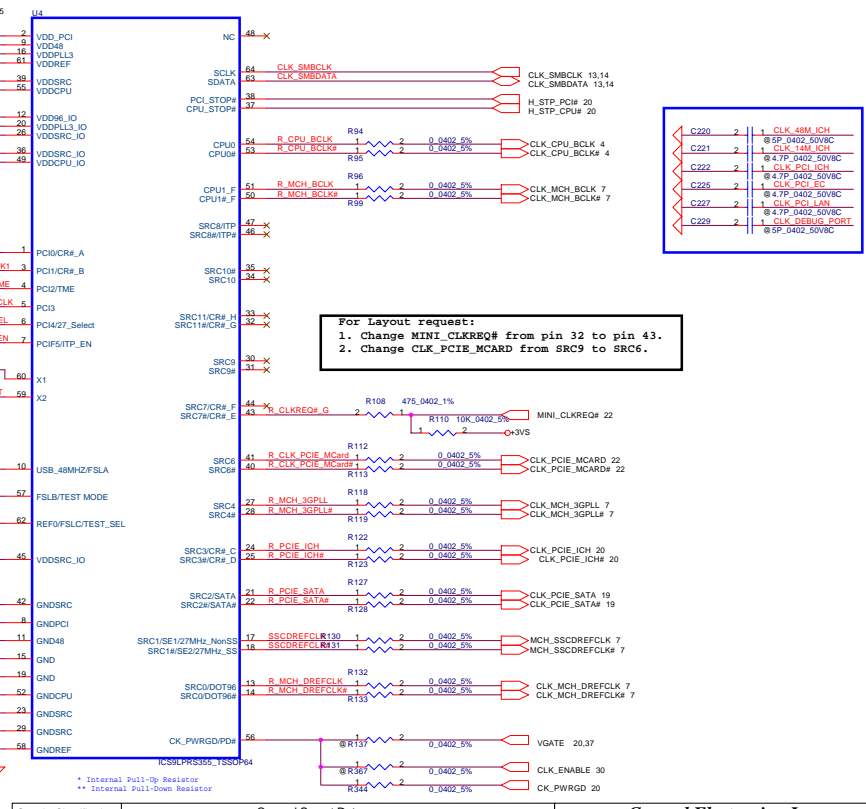
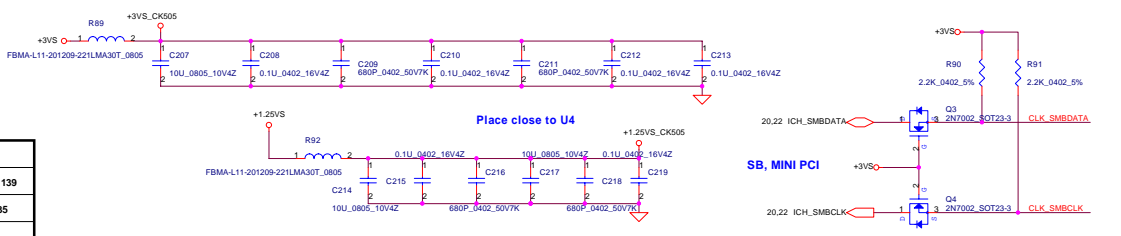
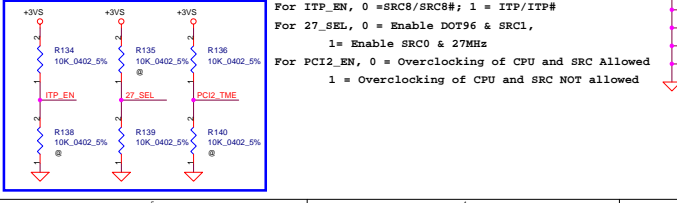
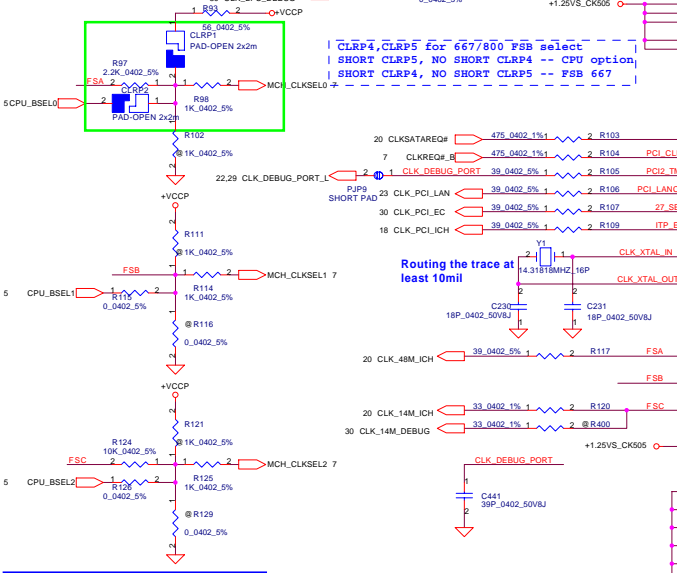
Compal Security Data				Title	
Security Classification	2007/03/26	Deciphered Date	2006/03/10	DDR2-SODIMM SLOT2	
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				LA-4031P	Rev 1.0
				Date: Wednesday, October 24, 2007	Sheet 14 of 42

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Set:

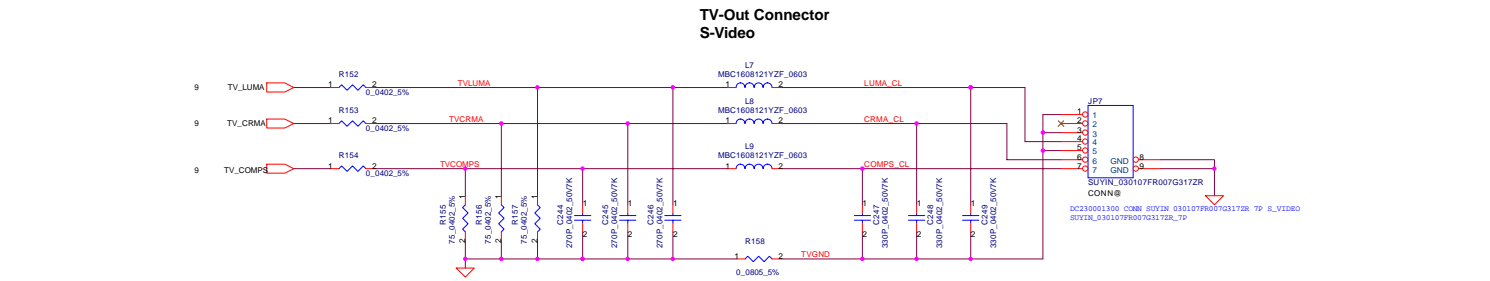
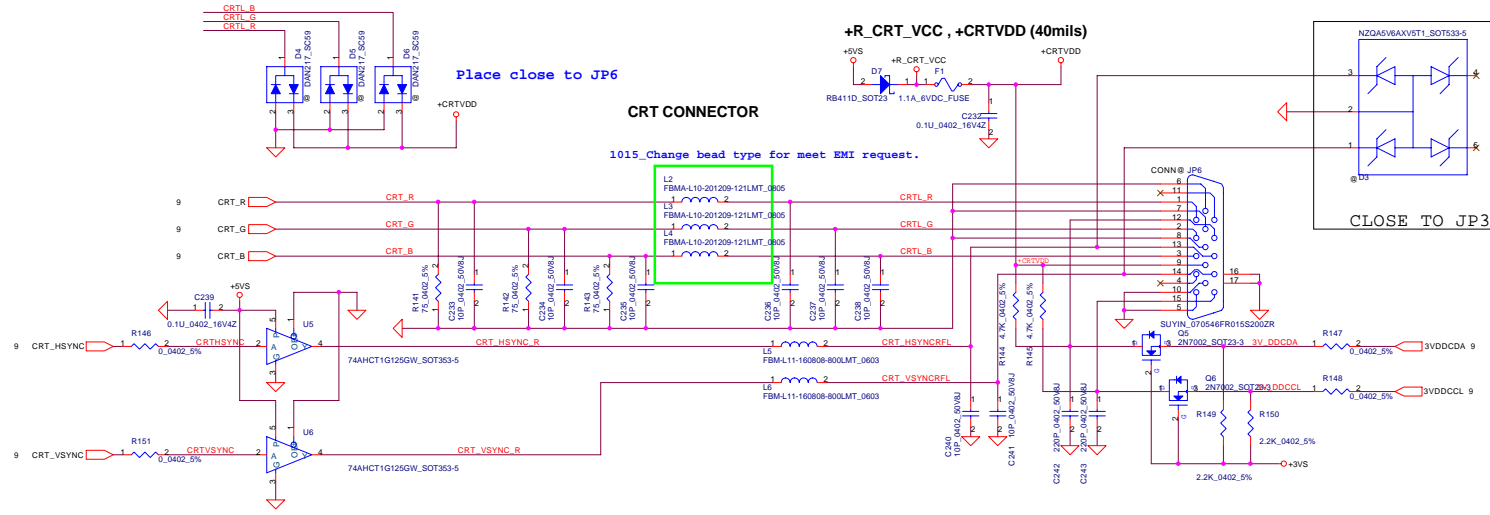
CPU Driven	Stuff	R107	R1135	R1083
*(Default)	No Stuff	R1074	R1086	R1098 R1113 R1128 R1139
	Stuff	R1086	R1139	R1135 R1074 R1139 R1135
667MHz	No Stuff	R1083	R1107	R1128 R1113 R1098
	Stuff	R1135	R1139	
800MHz	No Stuff	R1083	R1086	R1098 R1128 R1074 R1107 R1113
	Stuff	R1135	R1139	

1015_Change CLR1P and CLR2 type like the same as RJP4.

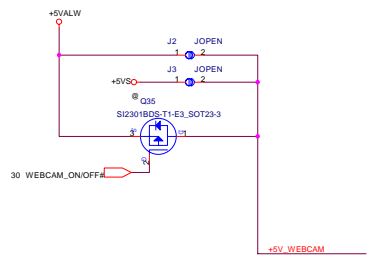


C220	2	1	CLK_48M_ICH
C221	2	1	5P_0402_50VBC
C222	2	1	CLK_14M_ICH
C222	2	1	4.7P_0402_50VBC
C225	2	1	CLK_PCIE_ICH
C225	2	1	4.7P_0402_50VBC
C227	2	1	CLK_PCIE_LAN
C227	2	1	4.7P_0402_50VBC
C229	2	1	CLK_DEBUG_PORT
C229	2	1	5P_0402_50VBC

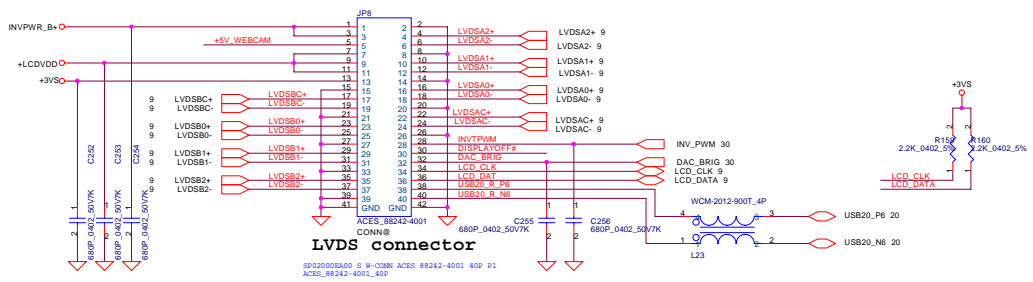
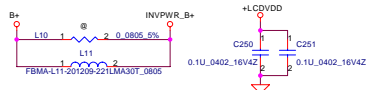
Security Classification	Compal Secret Data	Deciphered Date	2006/03/10	Title	Compal Electronics, Inc.
Issued Date	2007/03/26	Deciphered Date	2006/03/10		
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Size	Document Number	LA-4031P	Rev	1.0	
Date	Wednesday, October 24, 2007	Sheet	16	of	42



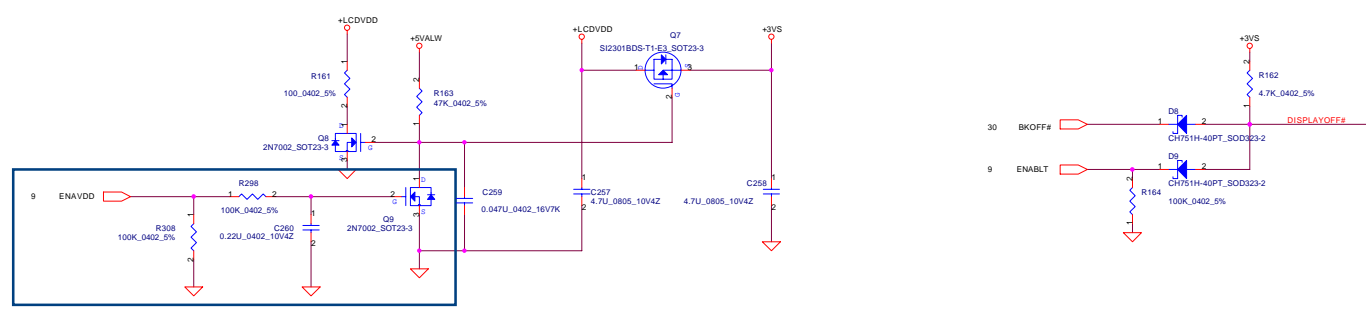
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Issued Date	2007/03/26	Deciphered Date	2006/07/26
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Title			Compal Electronics, Inc.
Size			CRT & TVout Connector
Document Number			LA-4031P
Date			Wednesday, October 24, 2007
Sheet			16 of 42
Rev			1.0



LVDS CONN

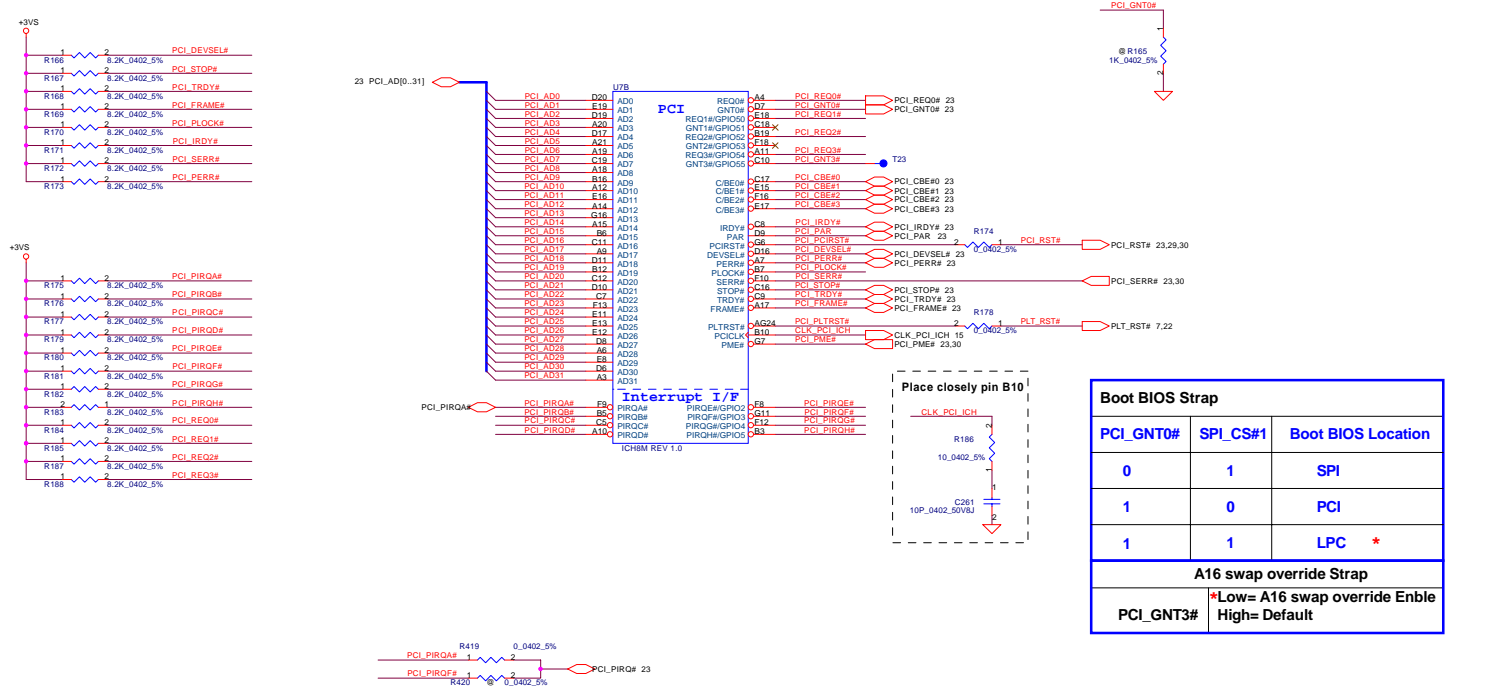


LVDS connector
 ACES_86242-4001
 CONNR
 680P_0402_50V7K
 C256 680P_0402_50V7K
 L23
 WCM-2012-900T_4P
 USB20_P6 20
 USB20_N6 20
 INV_PWM 30
 DAC_BRIG 30
 LCD_CLK 9
 LCD_DATA 9
 LVDSA2+ 9
 LVDSA2- 9
 LVDSA1+ 9
 LVDSA1- 9
 LVDSA0+ 9
 LVDSA0- 9
 LVDSB0+ 9
 LVDSB0- 9
 LVDSB1+ 9
 LVDSB1- 9
 LVDSB2+ 9
 LVDSB2- 9
 INV_PDM 28
 DISPLAYOFF# 28
 DAC_BRIG 30
 LCD_CLK 9
 LCD_DATA 9
 USB20_R_N6 38
 USB20_B_N6 40
 GND 41
 GND 42
 GND 39
 GND 40
 ACES_86242-4001
 CONNR
 680P_0402_50V7K
 C255
 680P_0402_50V7K
 L23
 WCM-2012-900T_4P
 USB20_P6 20
 USB20_N6 20
 INV_PWM 30
 DAC_BRIG 30
 LCD_CLK 9
 LCD_DATA 9
 LVDSA2+ 9
 LVDSA2- 9
 LVDSA1+ 9
 LVDSA1- 9
 LVDSA0+ 9
 LVDSA0- 9
 LVDSB0+ 9
 LVDSB0- 9
 LVDSB1+ 9
 LVDSB1- 9
 LVDSB2+ 9
 LVDSB2- 9
 INV_PDM 28
 DISPLAYOFF# 28
 DAC_BRIG 30
 LCD_CLK 9
 LCD_DATA 9
 USB20_R_N6 38
 USB20_B_N6 40
 GND 41
 GND 42
 GND 39
 GND 40

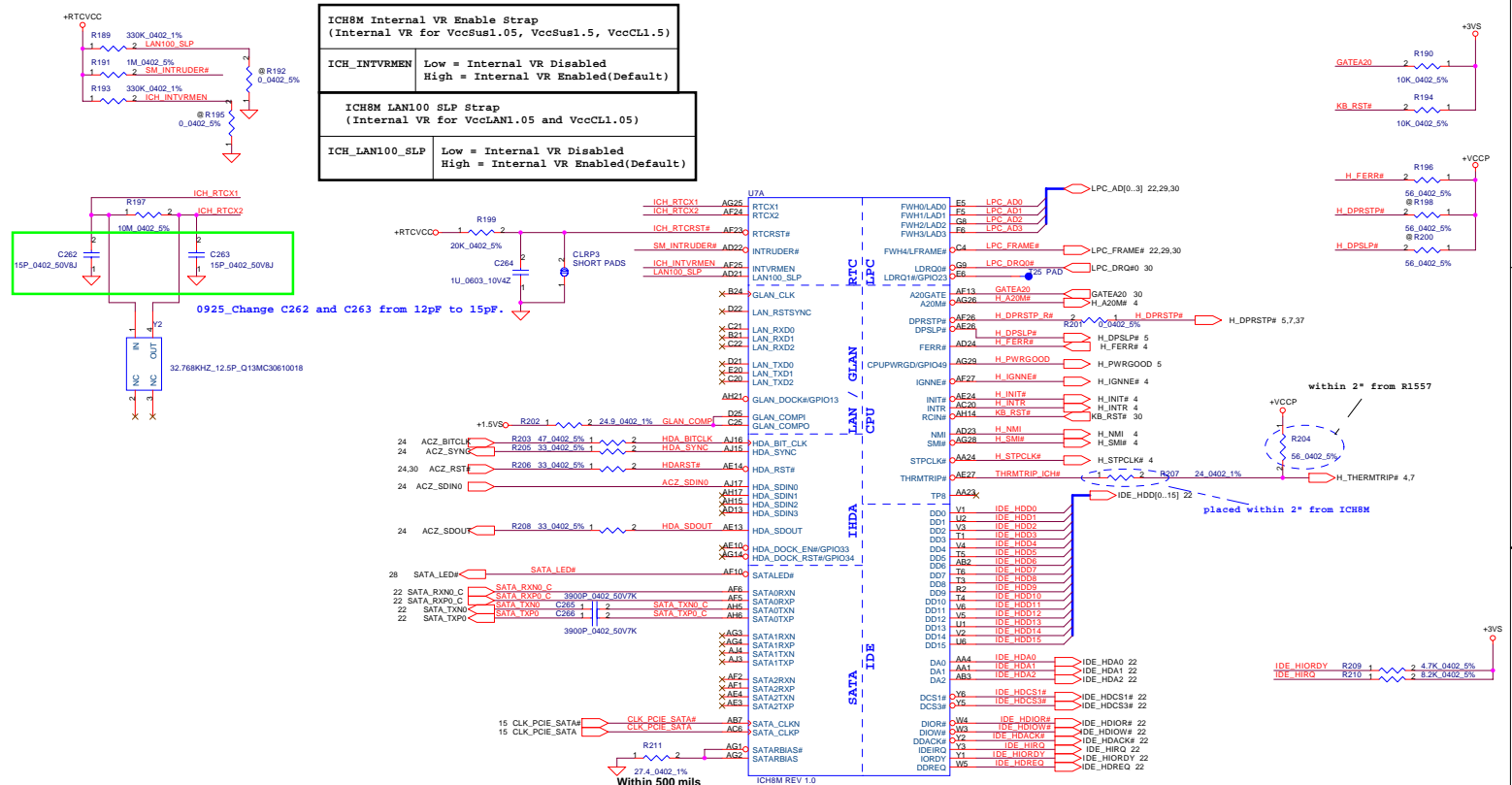


Avoid Panel display garbage after power on.

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Size	Document Number	Rev	Date: Wednesday, October 24, 2007 Sheet 17 of 42		
	LA-403P	1.0			

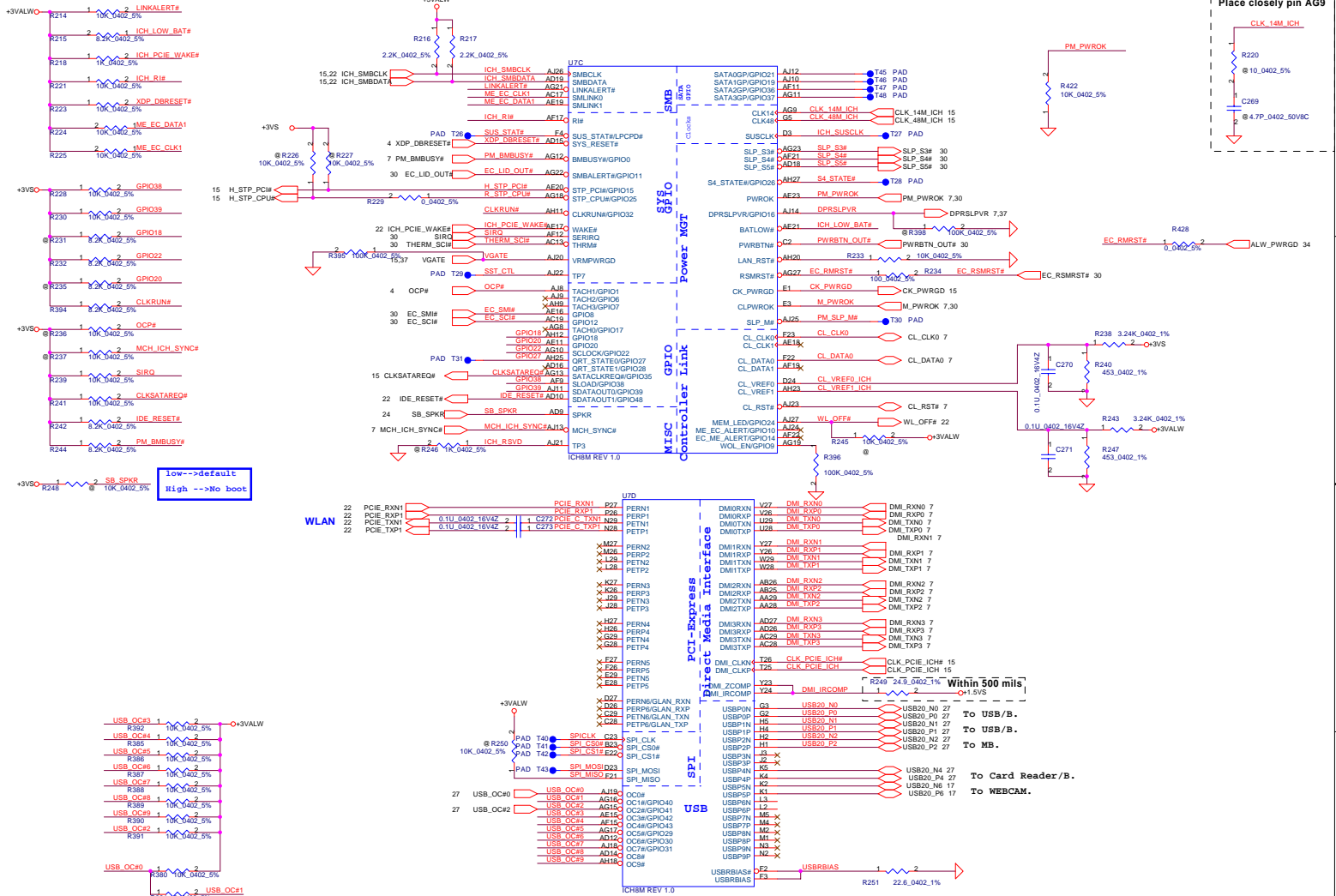


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Issued Date	2007/03/26	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
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				LA-4031P	Rev
Date	Wednesday, October 24, 2007	Sheet	18	of	42



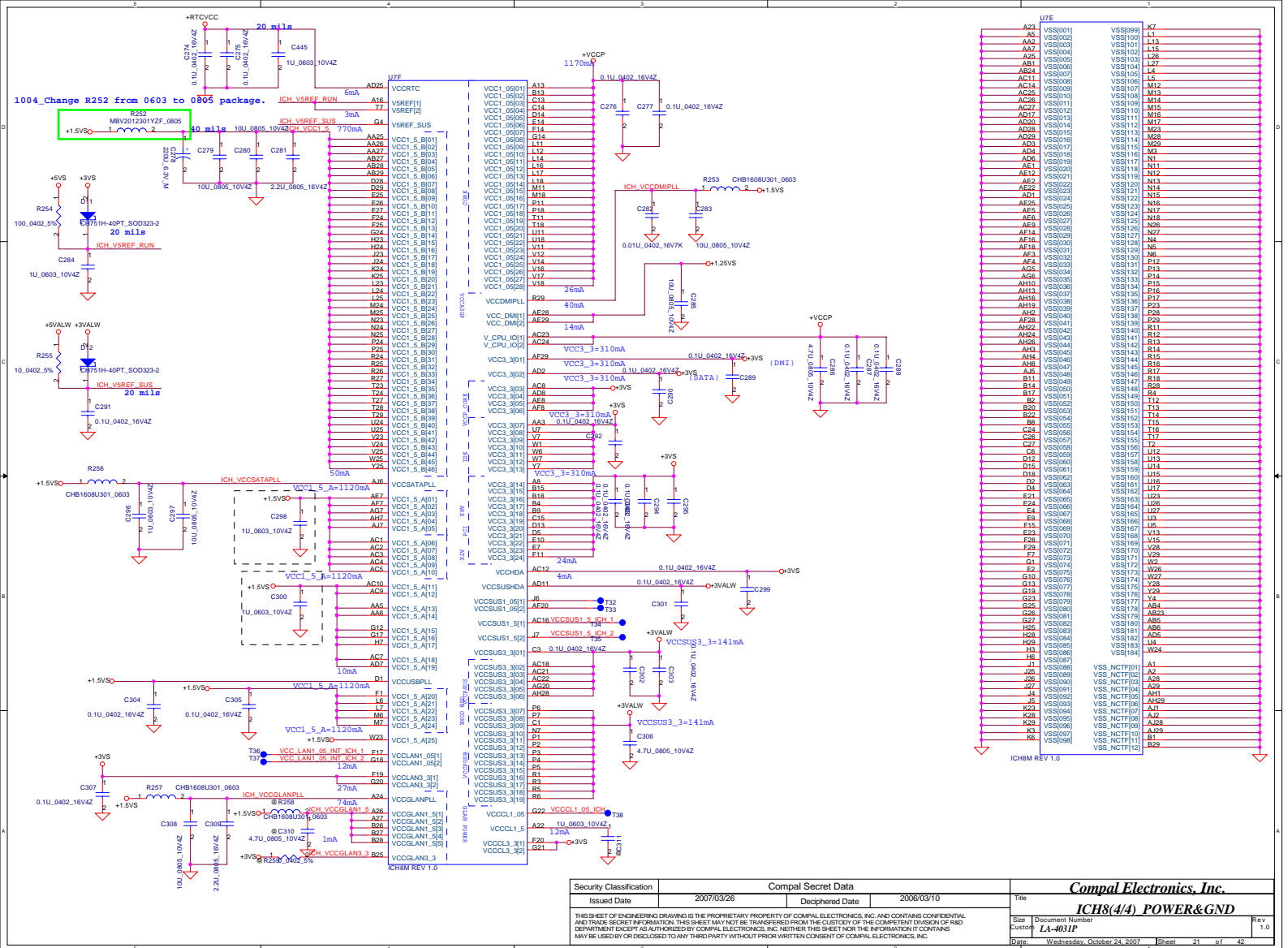
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Date	Wednesday, October 24, 2007	Sheet	18	of	42

Compal Electronics, Inc.
ICH8(2/4) LAN, HD, IDE, LPC



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Issued Date	2007/03/26	Deciphered Date	2006/03/10
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Size	Document Number	Rev	
Customer	LA-401P	1.0	
Date	Wednesday, October 24, 2007	Sheet	29 of 42

Compal Electronics, Inc.
ICH8(3/4) PM,USB,GPIO



Security Classification	Compal Secret Data		Date
Issued Date	2007/03/26	Deciphered Date	2006/03/10

Customer Information		Title	
Customer:	LA-401P	Title:	ICH8(4) POWER&GND
Date:	Wednesday, October 24, 2007	Sheet:	21 of 42

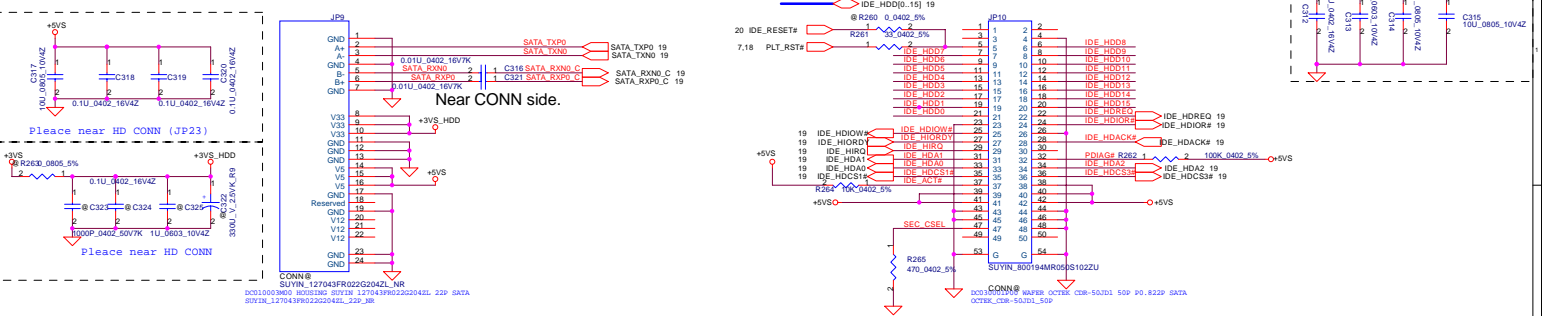
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Compal Electronics, Inc.
 ICH8(4) POWER&GND
 LA-401P
 Wednesday, October 24, 2007

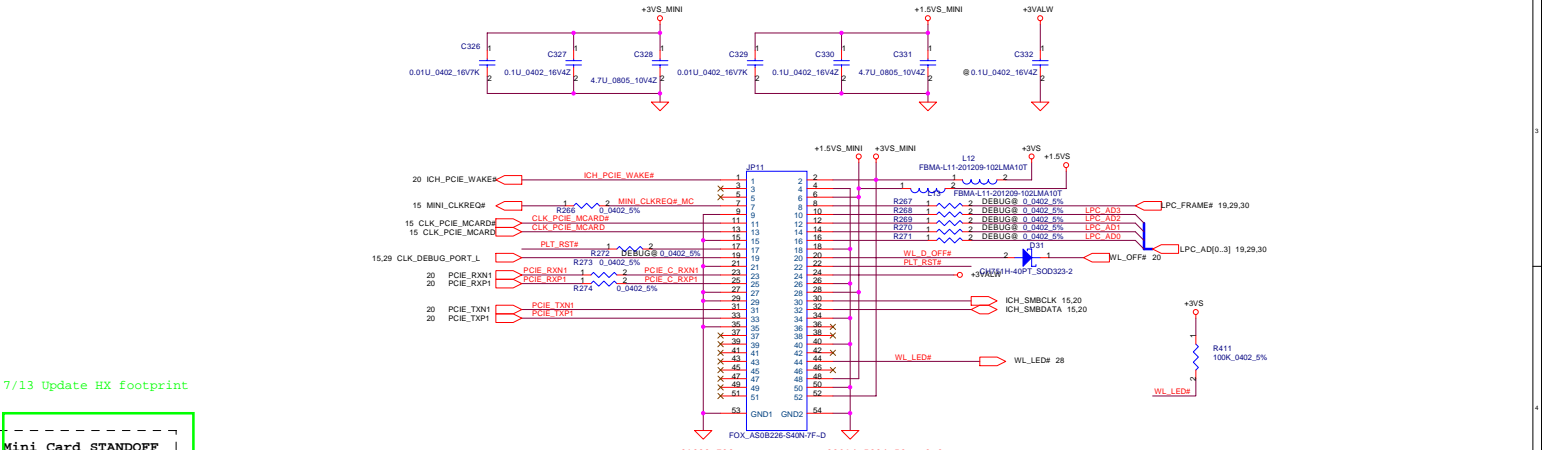
HDD Connector

CD-ROM Connector

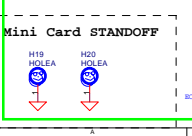
Place caps. near ODD CONN.



Mini-Express Card---WLAN

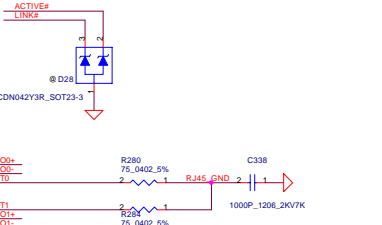
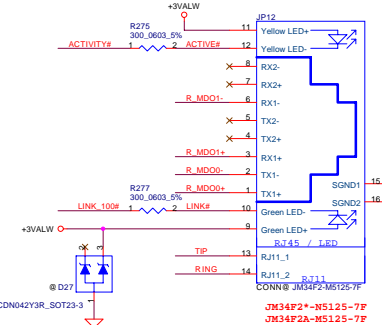
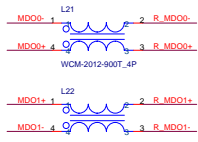


7/13 Update HX footprint

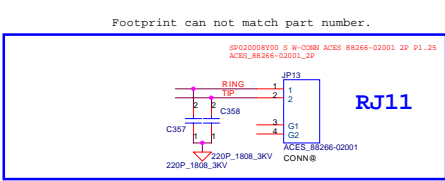
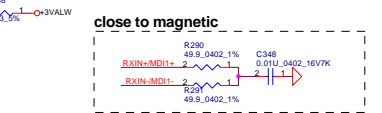
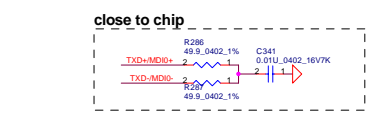
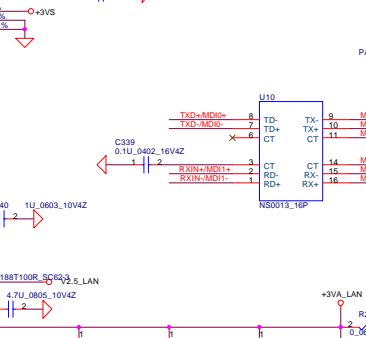
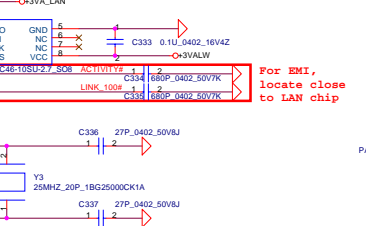
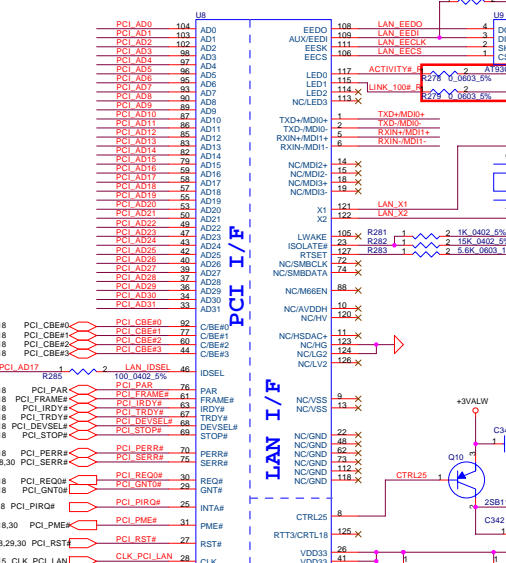


Security Classification	Compal Secret Data	
Issued Date	2007/03/26	Deciphered Date
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Title HDD/ODD/Mini Card CONN.		Date Wednesday, October 24, 2007
Size Document Number LA-4031P		Sheet 22 of 42
Rev 1.0		

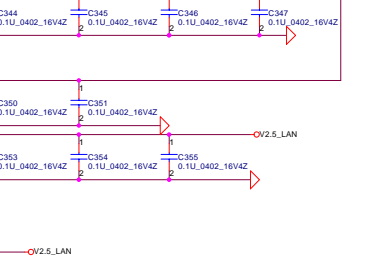
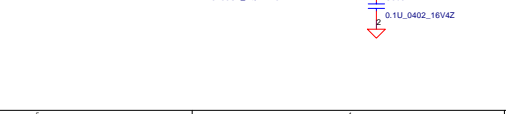
Closet to JP12.



18 PCI_AD[0..31]



Power



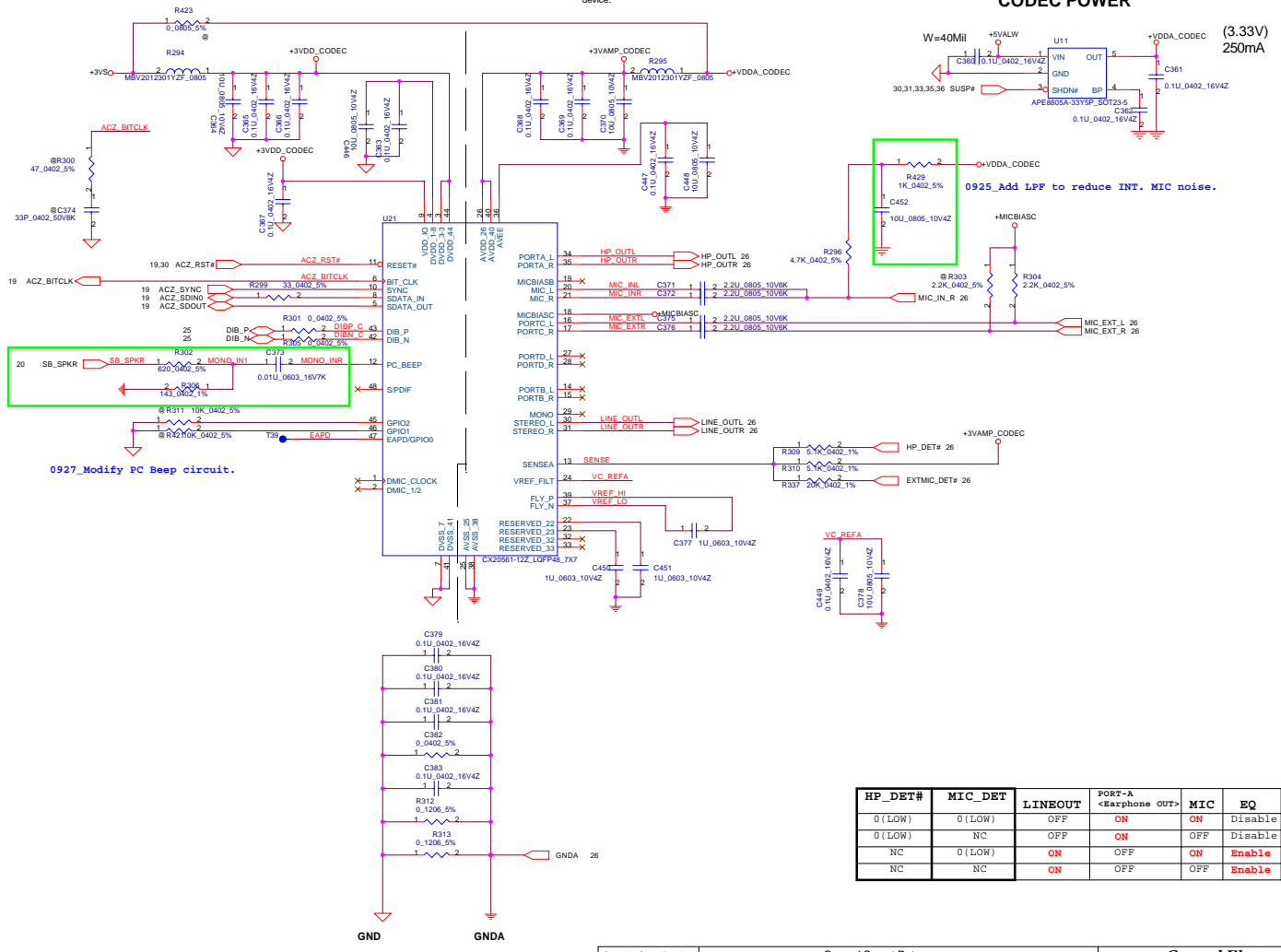
Security Classification				Compal Secret Data					
Issued Date	2007/03/26	Deciphered Date	2007/08/29	Title	LAN-8100CL				
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Date	Wednesday, October 24, 2007	Sheet	23	of	42				

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

AUDIO CODEC

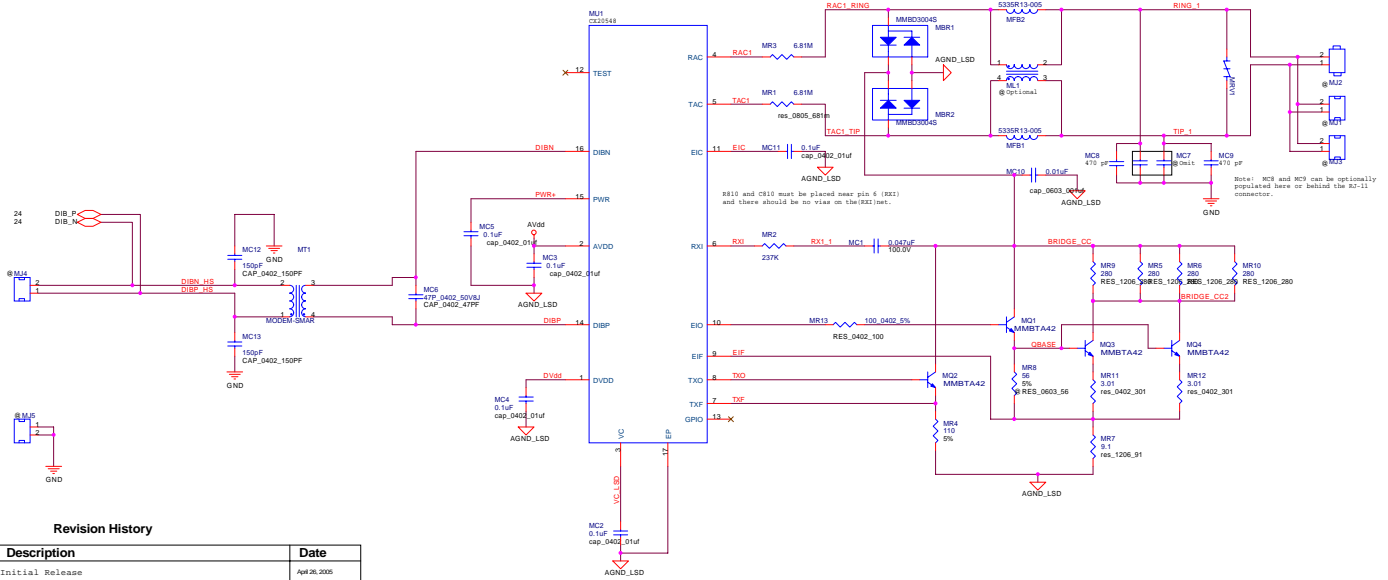
For Layout:
Place decoupling caps near the power pins of SmartAMC device.

CODEC POWER



HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

Security Classification		Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Title	AMOM codec		
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				Customer	LA-403P		
				Date	Wednesday, October 24, 2007	Sheet	24 of 42

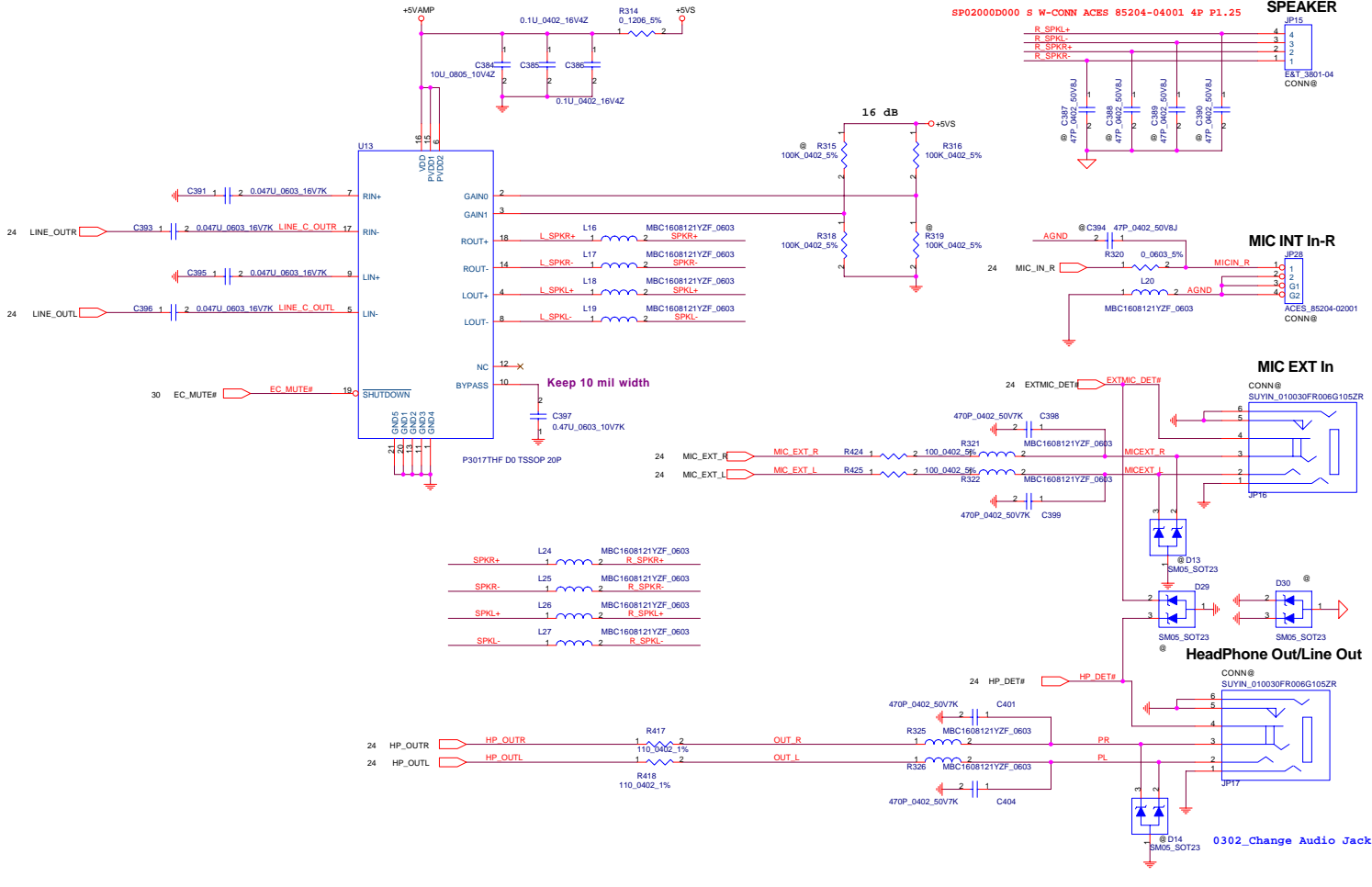


Note: MC8 and MC9 can be optionally populated here or behind the 82-11 connector.

Revision History

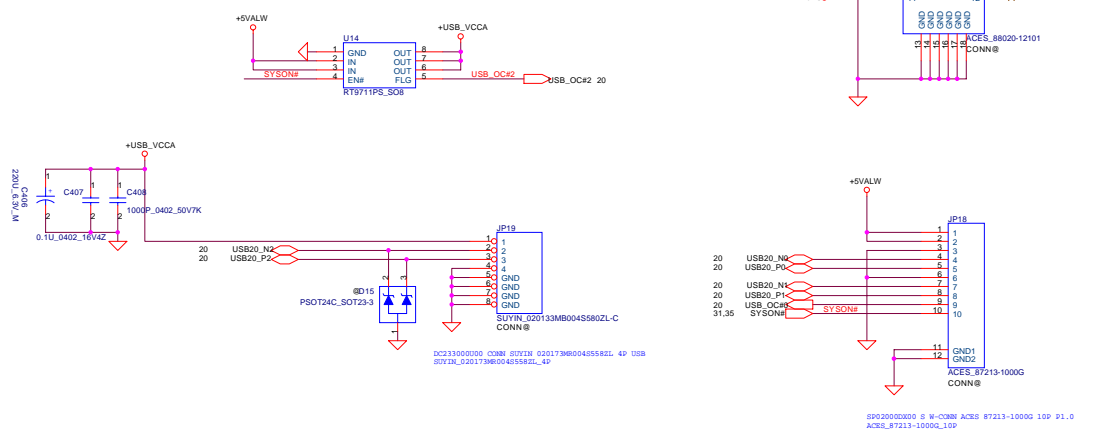
REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	April 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

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REV	DESCRIPTION	DATE	BY
1.0	LA-401P		
Date: Wednesday, October 24, 2007			Sheet 25 of 42



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				LA-403IP	Rev 1.0
				Date	Wednesday, October 24, 2007
				Sheet	26 of 42

USB Port

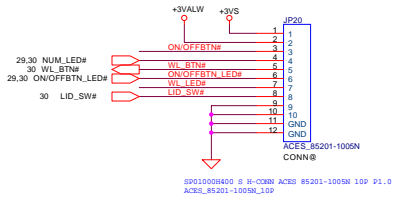


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Date: Wednesday, October 24, 2007			Sheet	27 of 42

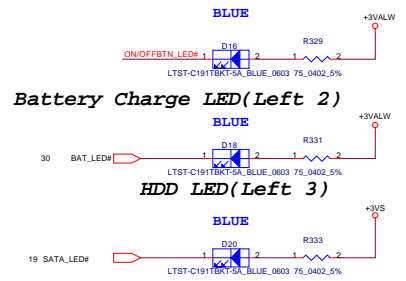
1015_Remove U22 and U23.



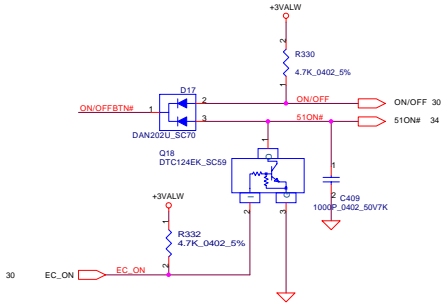
M/BtoS/B



POWER LED(Left 1)

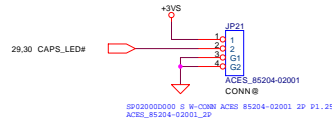


Power ON/OFF

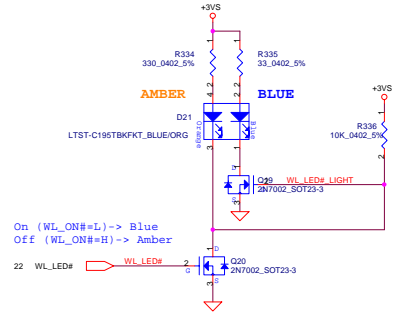


0426_Change all LED power source from 5V to 3V.

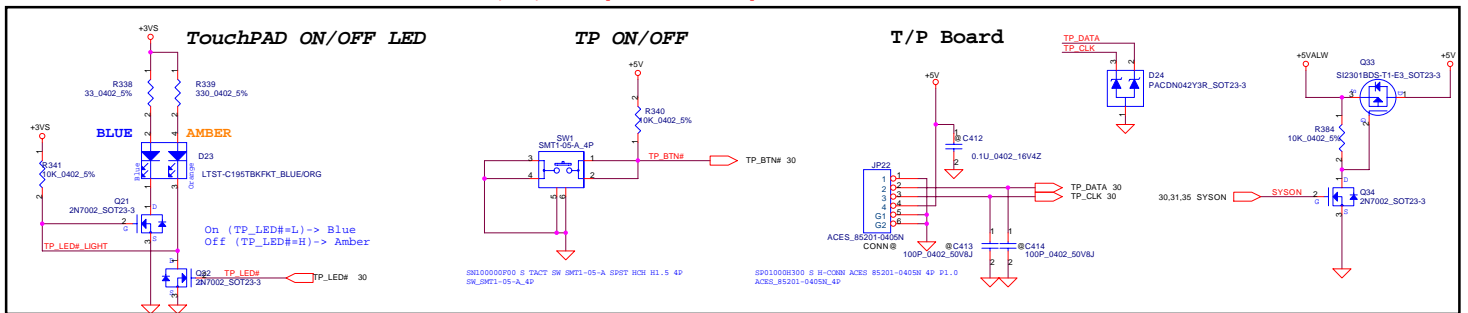
M/B to SB(Caps Lock LED)



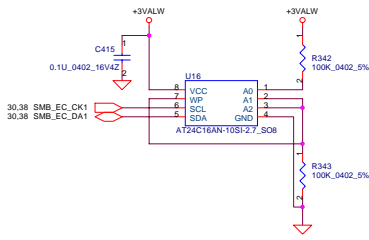
Wireless ON/OFF LED(Left 4)



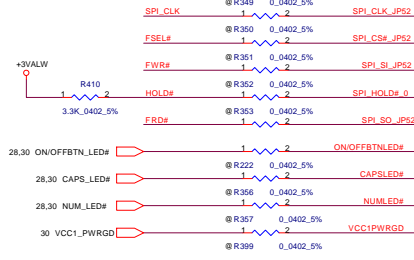
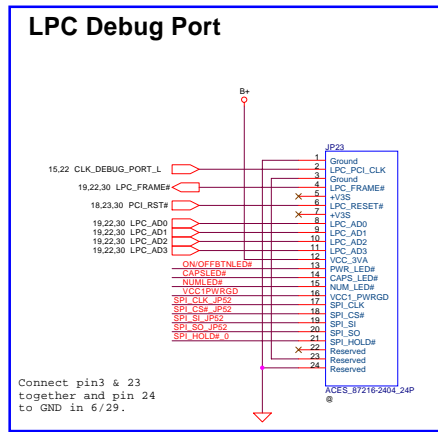
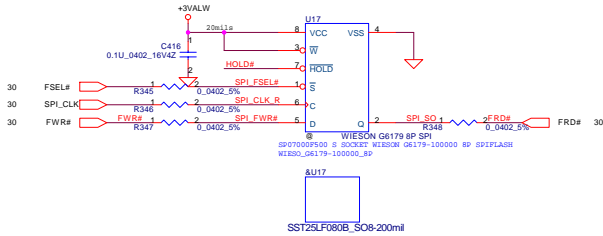
D21, D25, D23 Footprint can not match part number.



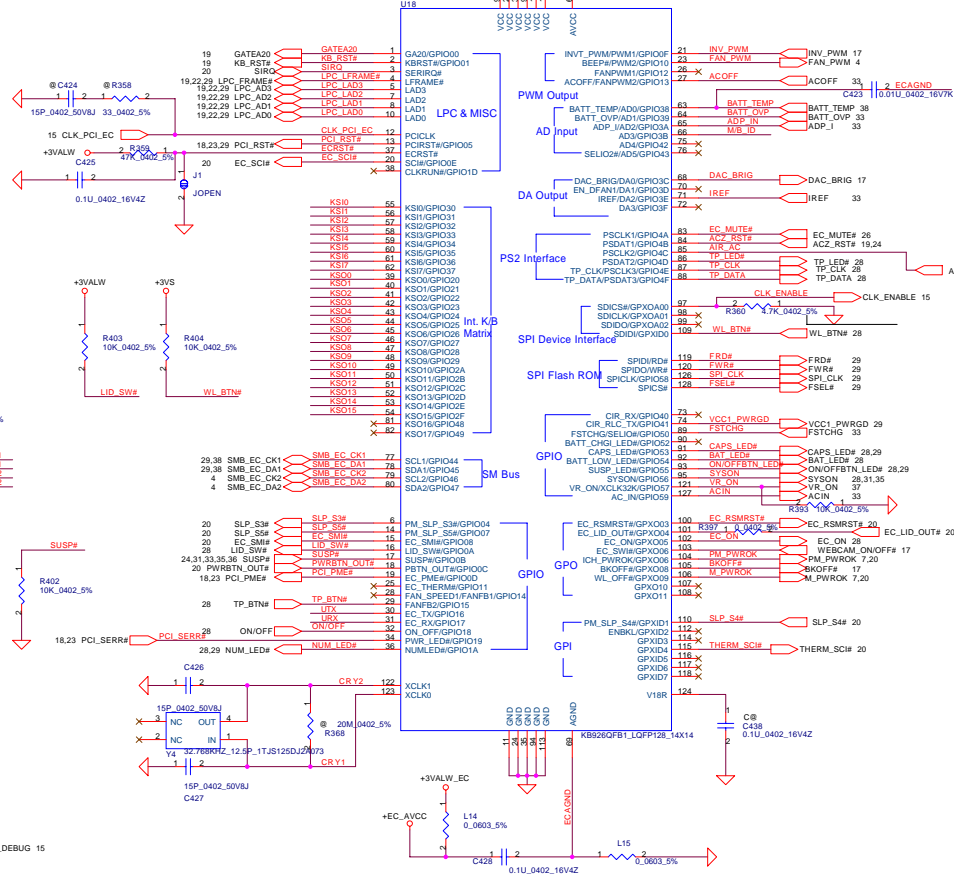
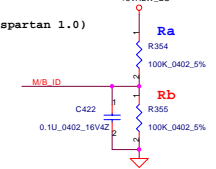
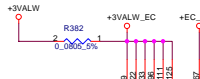
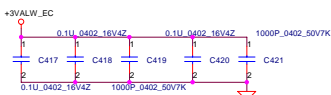
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/03/26	Deciphered Date	2006/07/26	Title
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				Rev: 1.0



SPI ROM

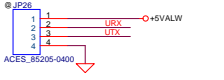


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Date	Wednesday, October 24, 2007	Sheet	29	of 42

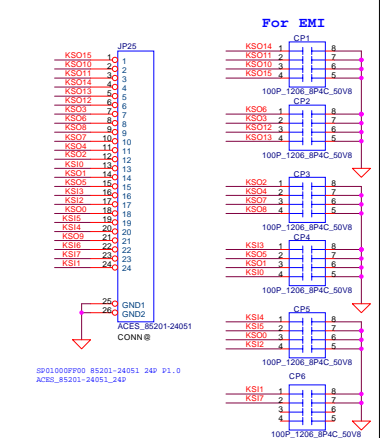
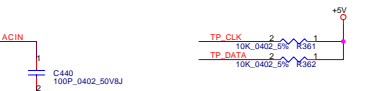
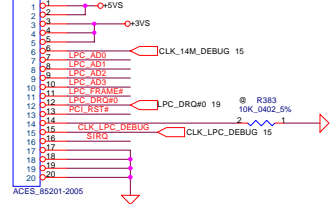


VCC	3.3V+/-5%							
Ra	100K+/-5%							
Board ID	Rb	V_min	V_max	V_min	V_max	typ	V_min	V_max
		AD_252	AD_252	AD_252	AD_252		AD_252	AD_252
0	1	8.2K+/-5%	0.216V	0.250V	0.289V			
2	2	1.8K+/-5%	0.436V	0.503V	0.538V			
3	3	33K+/-5%	0.712V	0.819V	0.875V			
4	4	56K+/-5%	1.036V	1.185V	1.264V			
5	5	100K+/-5%	1.453V	1.650V	1.759V			
6	6	200K+/-5%	1.935V	2.200V	2.341V			
7	7	NC	2.500V	3.300V	3.300V			

EC DEBUG port

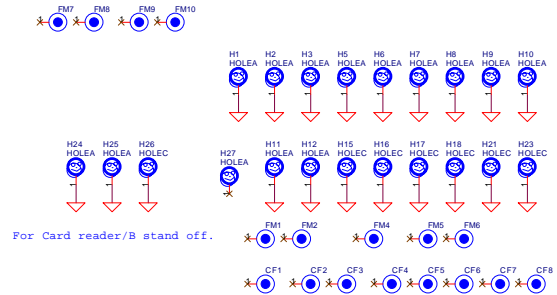
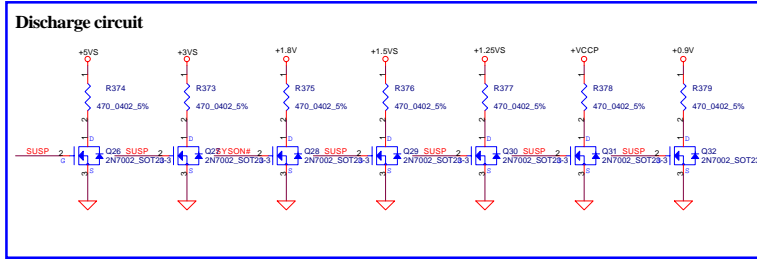
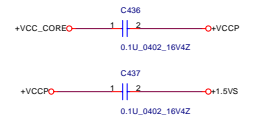
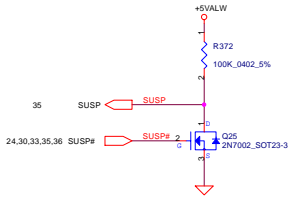
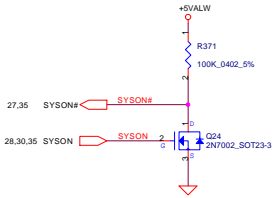
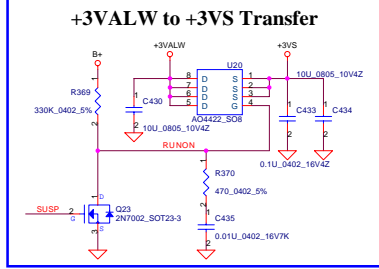
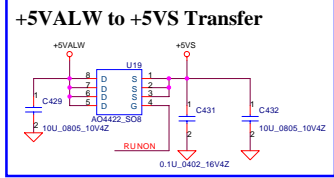


FOR LPC SIO DEBUG PORT

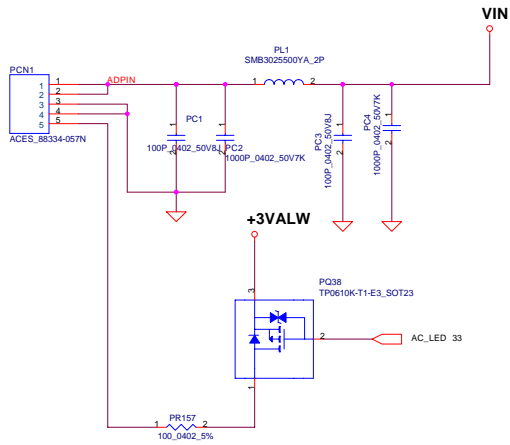


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Issued Date	2007/03/26	Deciphered Date			

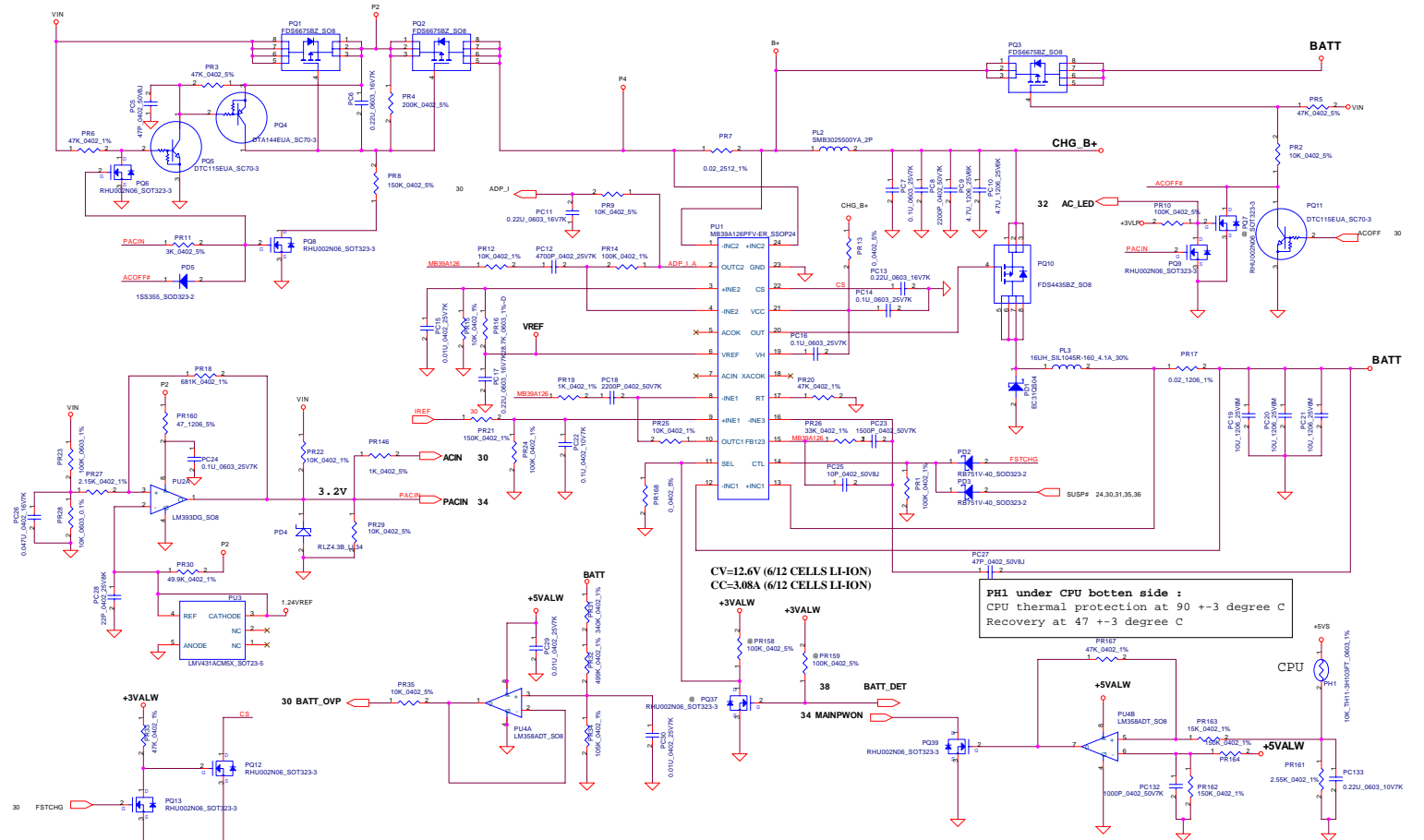
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Size	Document Number	LA-4031P		Rev	1.0
Date	Wednesday, October 24, 2007	Sheet	31	of	42

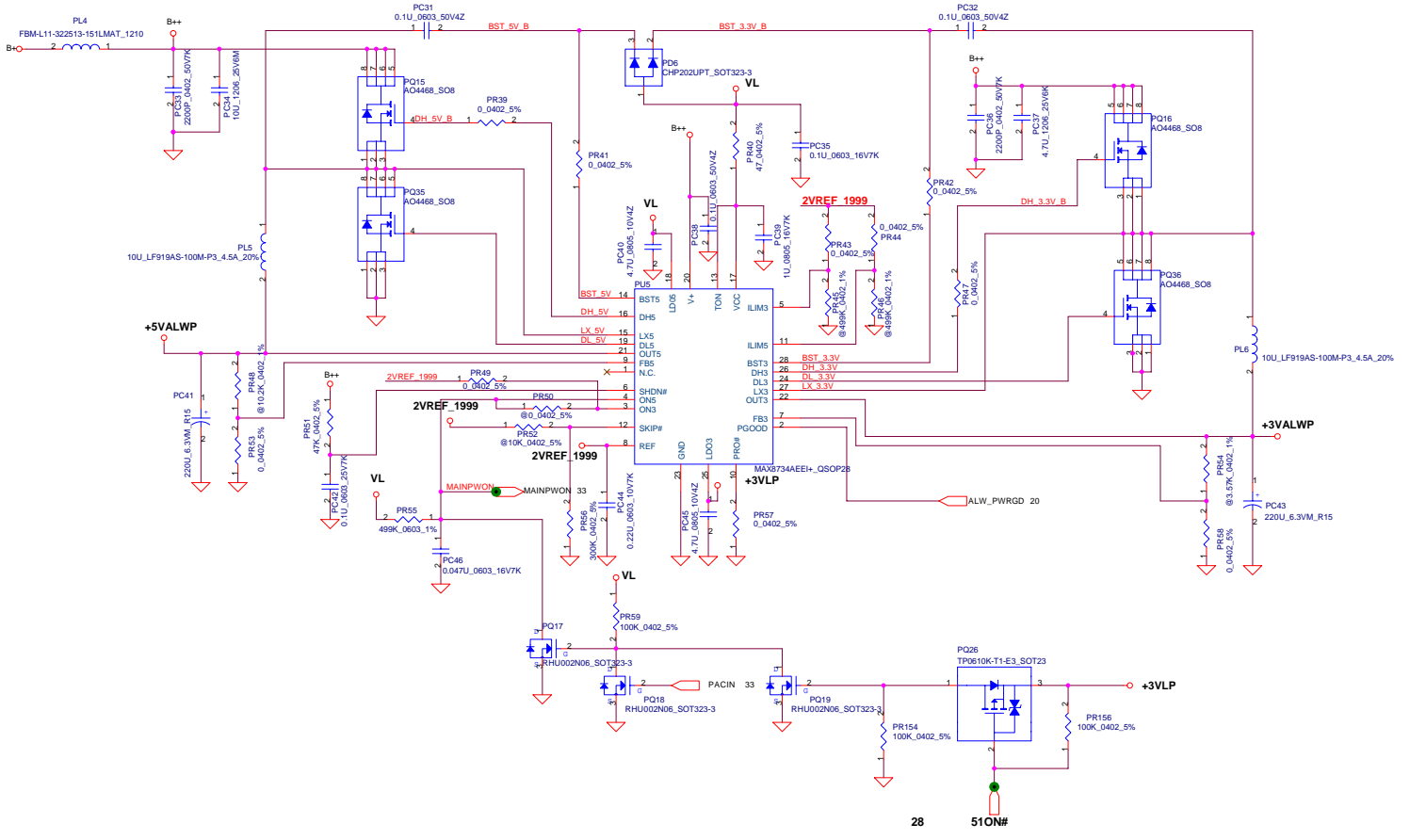


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Date	Wednesday, October 24, 2007	Sheet	32	of 42

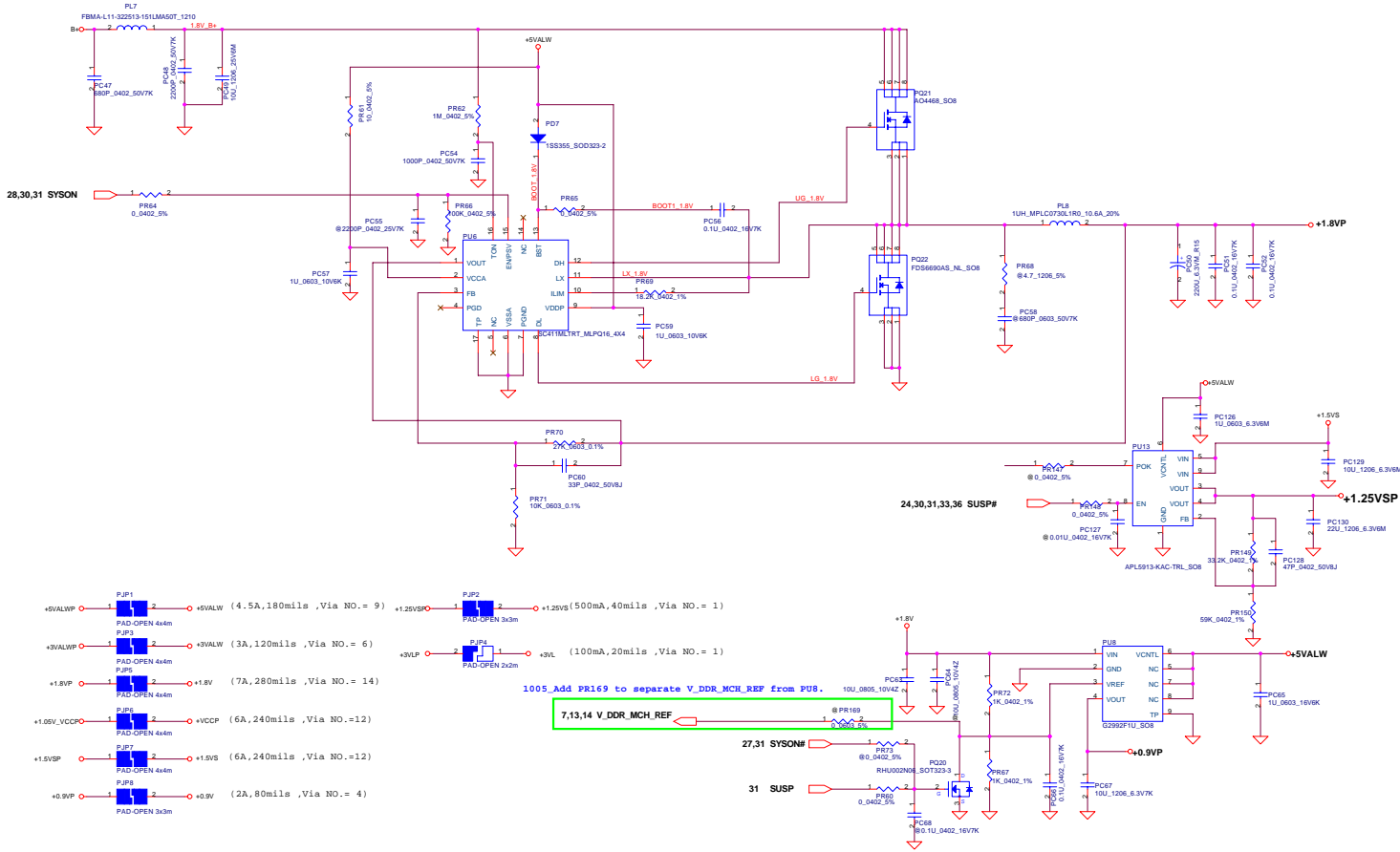


PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 47 +/-3 degree C

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DATE	WSP202509_24_0909	ISSUED	53 OF 42

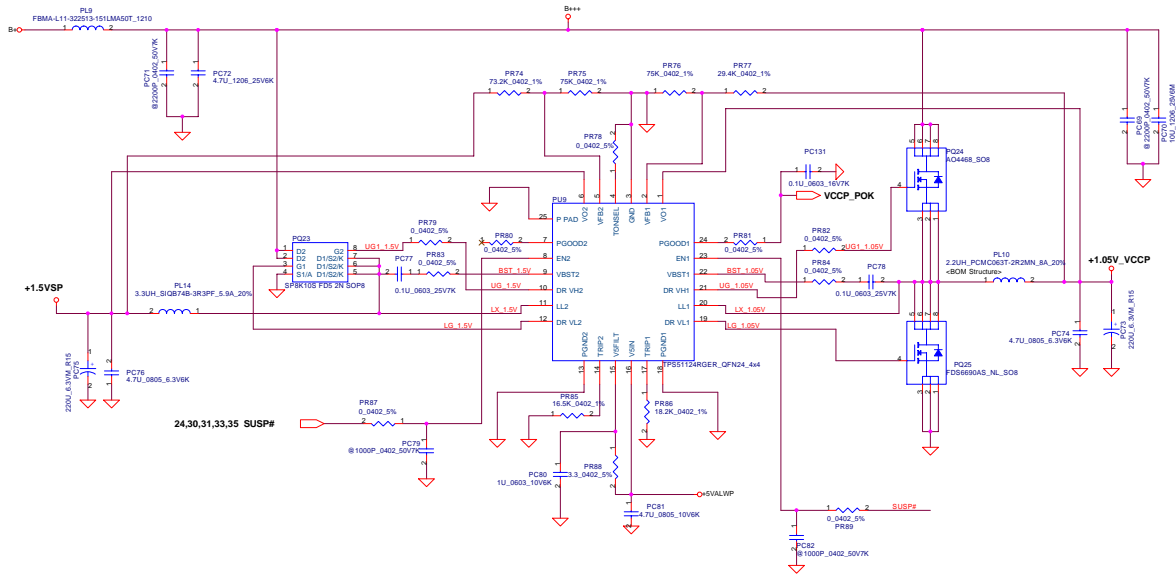


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Date:	Wednesday, October 24, 2007	Sheet:	34	of 42	

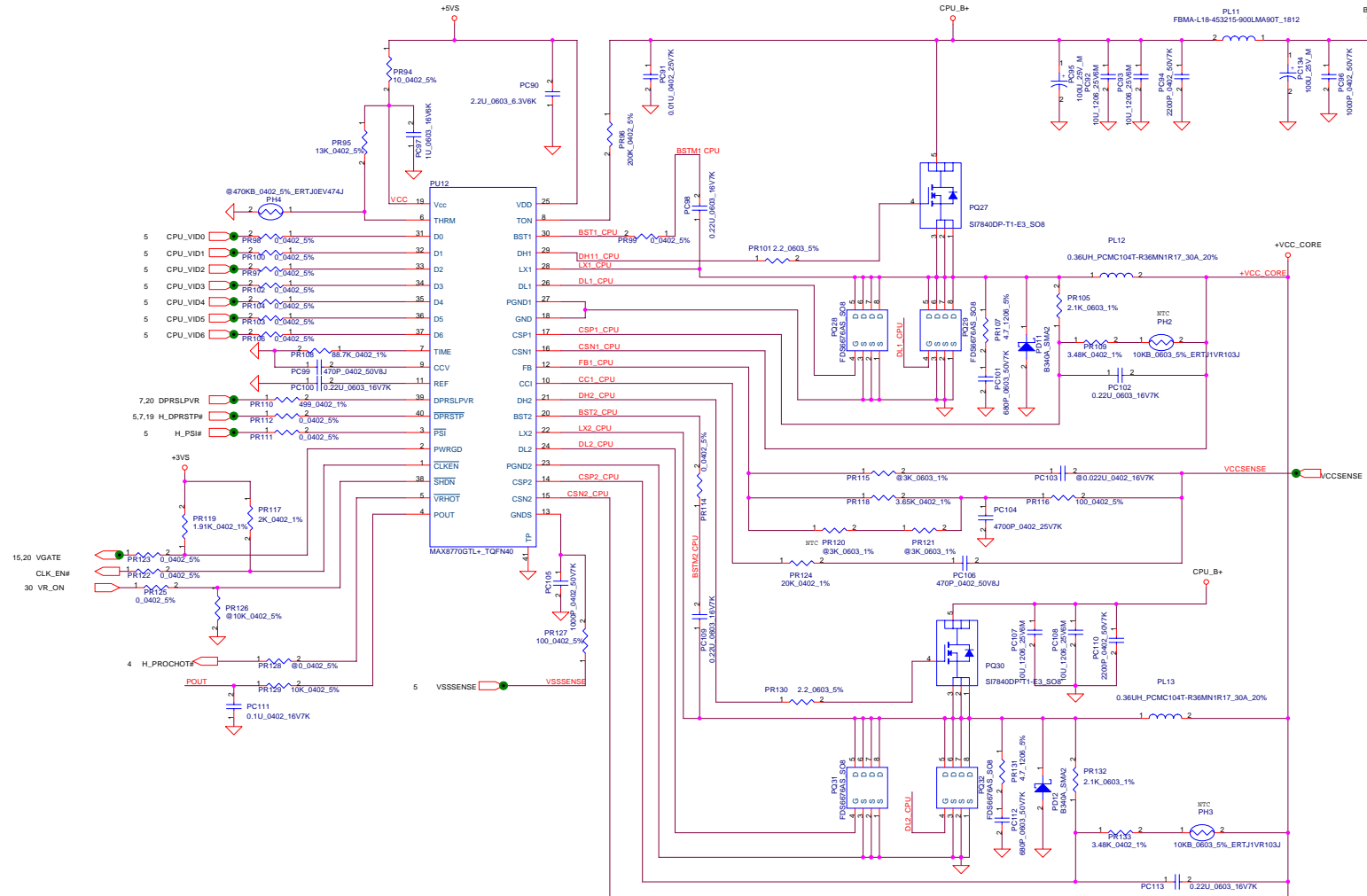


- +SVALW PJP1 2 +SVALW (4.5A,180mils ,Via NO.= 9)
- +SVALW PJP2 2 +SVALW (3A,120mils ,Via NO.= 6)
- +1.8VP PJP3 2 +1.8V (7A,280mils ,Via NO.= 14)
- +1.05V_VCCP PJP6 2 +VCCP (6A,240mils ,Via NO.=12)
- +1.5VSP PJP7 2 +1.5VS (6A,240mils ,Via NO.=12)
- +0.9VP PJP8 2 +0.9V (2A,80mils ,Via NO.= 4)
- +1.25VSP PJP9 2 +1.25VS (500mA,40mils ,Via NO.= 1)
- +9VP PJP10 2 +9V (100mA,20mils ,Via NO.= 1)

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Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>	Title	1.8VP/0.9VSP/2.5VSP
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Size	Document Number:	LA-403P		Rev	1.0
Date	Wednesday, October 28, 2009	Issue	35	of	49

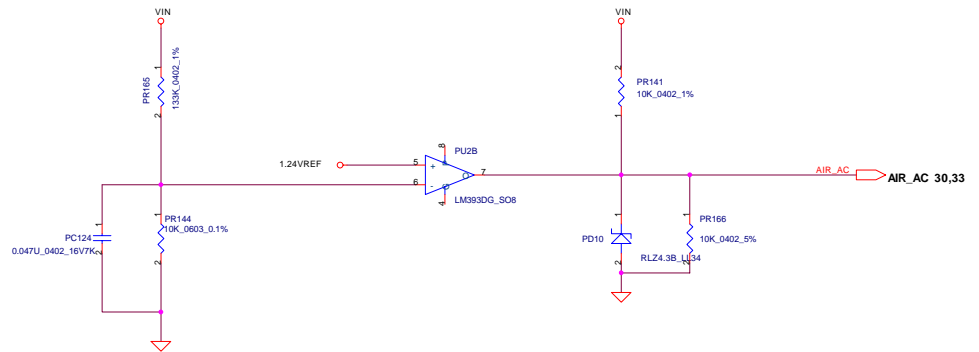
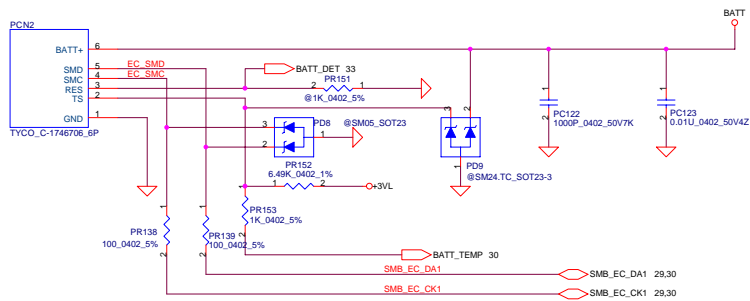


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Compal Electronics, Inc.		
File	+CPU CORE	
Site	Document Number	Rev
Client	10KB_0603_5%_ERTJ1VR103J	1.0
Date	Wednesday, October 24, 2007	Sheet 37 of 42



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				Size	Document Number
		Date: Wednesday, October 24, 2007		Sheet 42 of 38	

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

Security Classification	Compal Secret Data		Title	
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				Size
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Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page	Date	Phase
1	Change R296 2.2K to 4.7K and Reserved R303	24	8/6	SI-->PV
2	Add R424 R425 100ohm on MIC_EXT_R and MIC_EXT_L	26	8/6	SI-->PV
3	Fine tune R298 C260 value	17	8/6	SI-->PV
4	Change PIRQ from F to A	18	8/14	SI-->PV
5	Connect PCI_SERR# to EC GPIO pin.	18	8/31	SI-->PV
6	Modify PC BEEP circuit.	20	8/31	SI-->PV
7	For support Intel Penryn CPU.	04	9/3	SI-->PV
8	For ESD request.	28	9/3	SI-->PV
9	For EMI request.	26	9/5	SI-->PV
10	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	26	9/7	SI-->PV
11	Add R417 and R418 to fine-tune Vp-p.	26	9/7	SI-->PV
12	For ESD request.	20	9/7	SI-->PV
13				
14				
15				
16				
17				
18				
19				
20				
21				
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Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page	Date	Phase
1	Solve Vref miss when entry S3 mode.	7	9/25	PV-->MV
2	Solve wave ripple on CRT and TV.	10	9/25	PV-->MV
3	Solve RTC timing too exceed.	18	9/25	PV-->MV
4	Reduce INT_MIC noise.	24	9/25	PV-->MV
5	Solve S3 resume fail when use Micron DDR module.	35	10/05	PV-->MV
6	Solve pop noise when entry or resume from S3.	24	9/27	PV-->MV
7	Solve EMI fail for Memory module.	7	9/27	PV-->MV
8	ICH 1.5V power rail 700mA current requirement.	21	10/04	PV-->MV
9	Remove U22 and U23.	28	10/15	PV-->MV
10	For EMI request.	16	10/15	PV-->MV
11	To avoid too easy to open solder for CLRP2.	15	10/15	PV-->MV
12	Solve acoustic noise issue.	10	10/22	PV-->MV
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