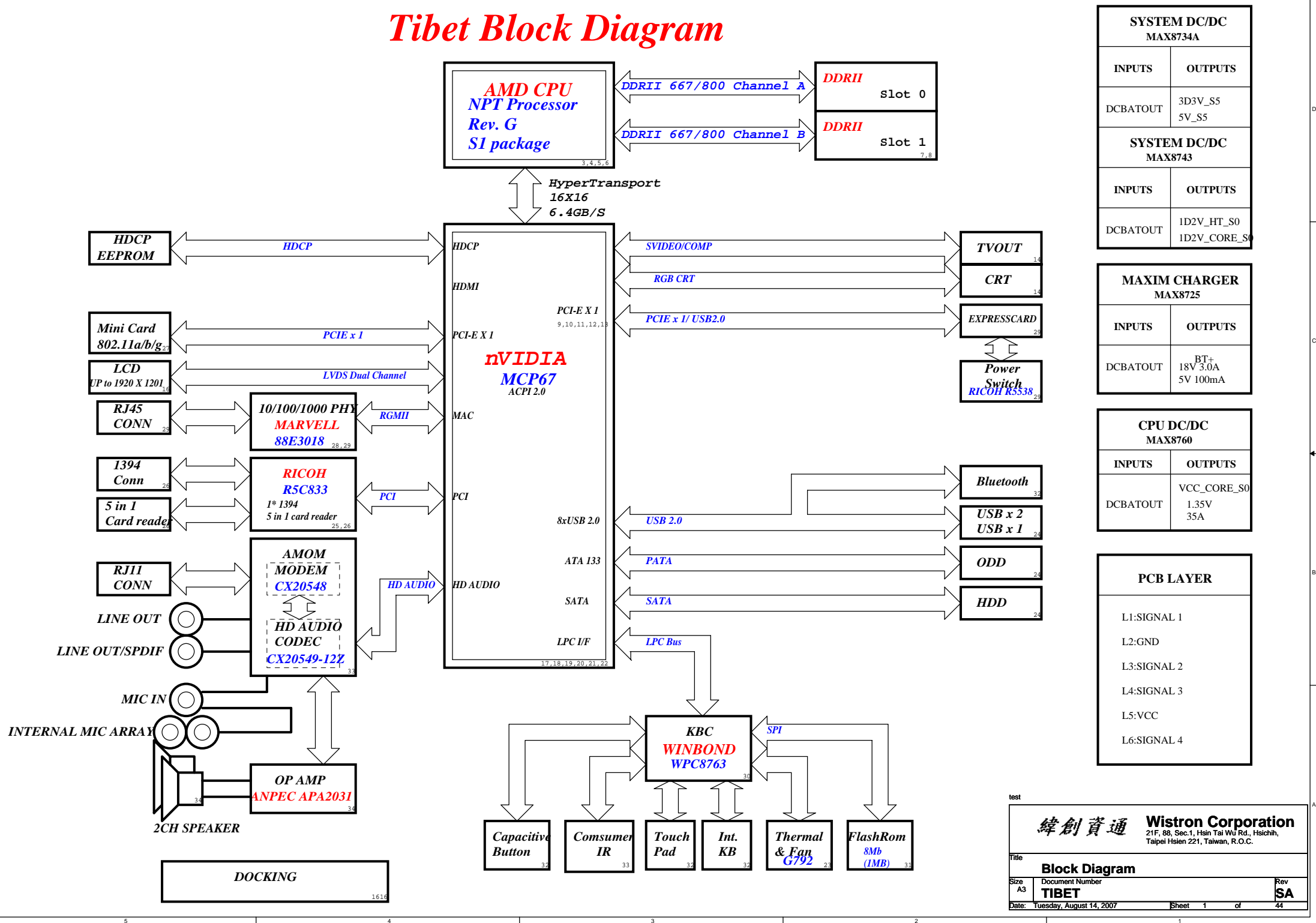


Tibet Block Diagram



SYSTEM DC/DC MAX8734A	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5
SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D2V_HT_S0 1D2V_CORE_S0

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8760	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 1.35V 35A

PCB LAYER	
L1: SIGNAL 1	
L2: GND	
L3: SIGNAL 2	
L4: SIGNAL 3	
L5: VCC	
L6: SIGNAL 4	

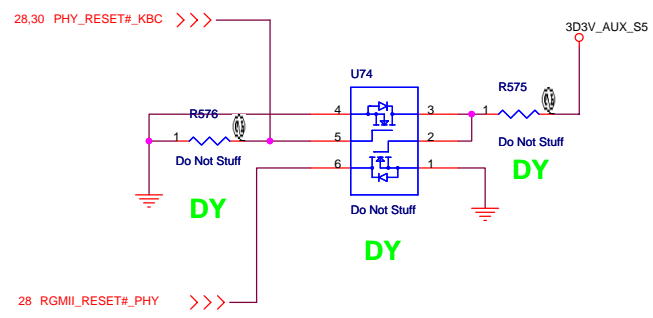
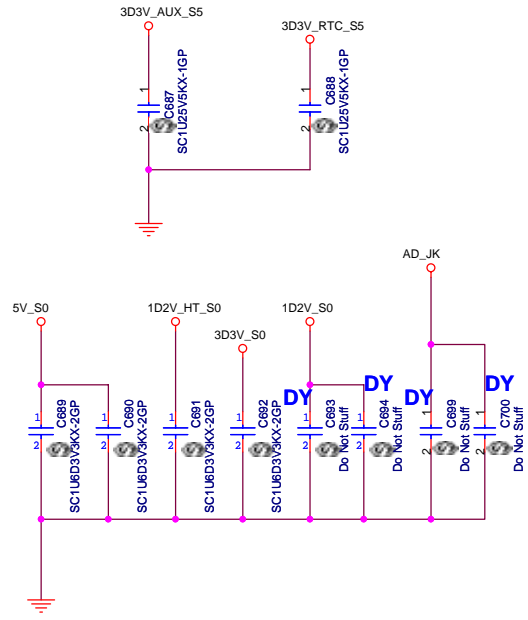
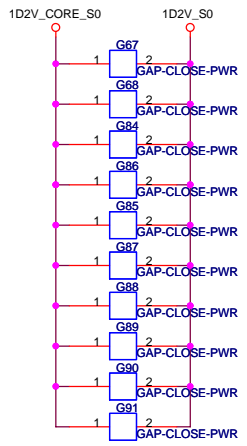
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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size: A3 Document Number: **TIBET** Rev: SA

Date: Tuesday, August 14, 2007 Sheet 1 of 44



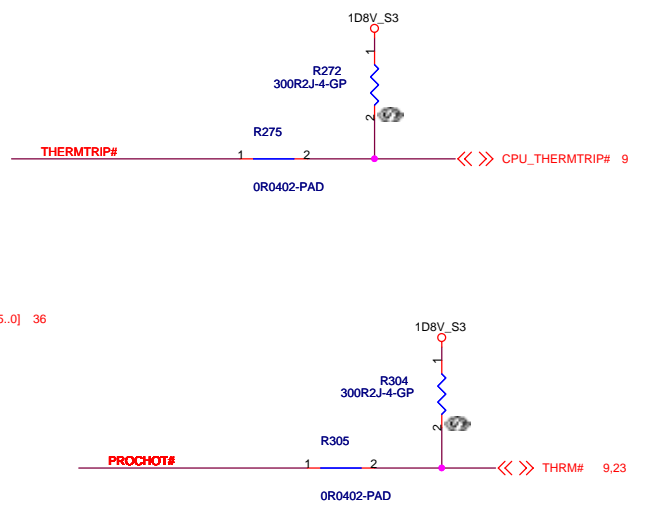
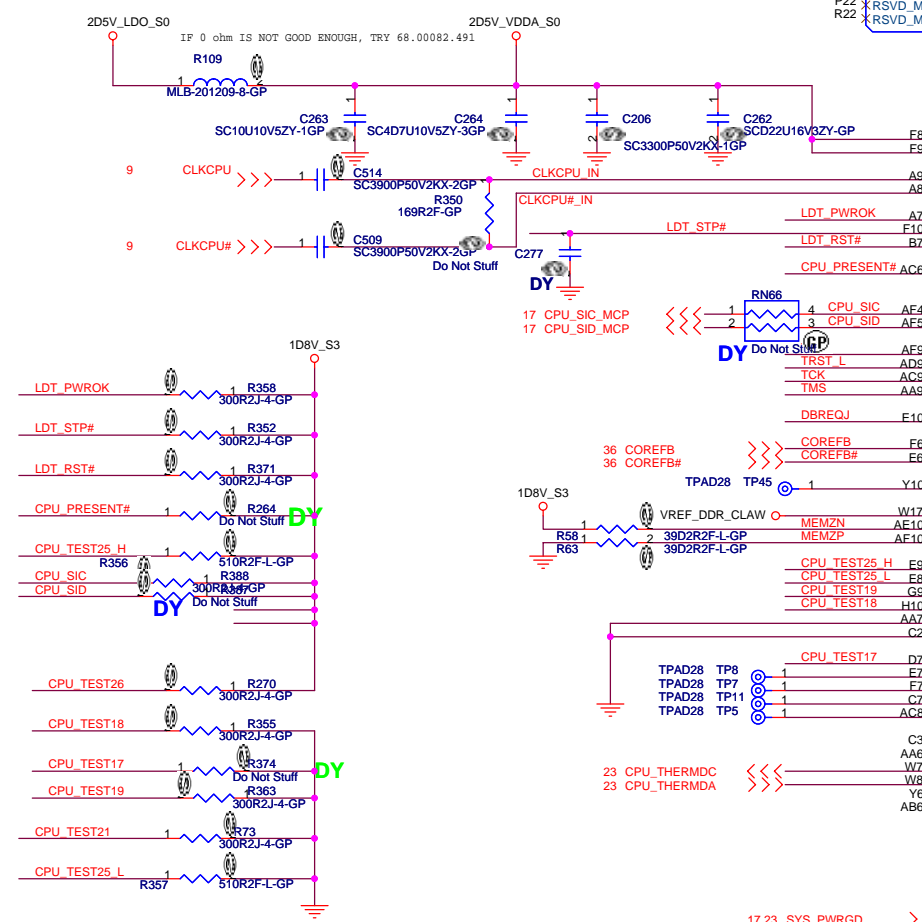
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緯創資通		Wistron Corporation	
		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			
Size A3	Document Number TIBET		Rev SA
Date: Tuesday, August 14, 2007		Sheet 2	of 44

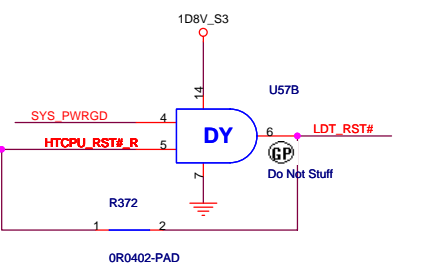
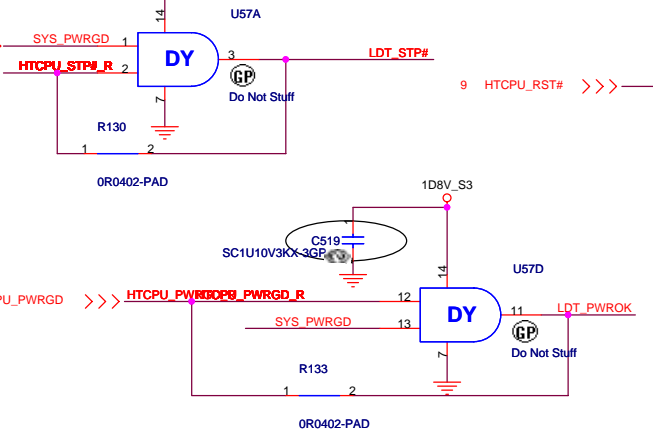
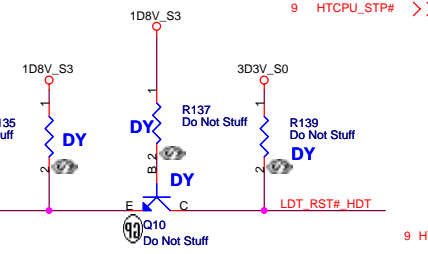
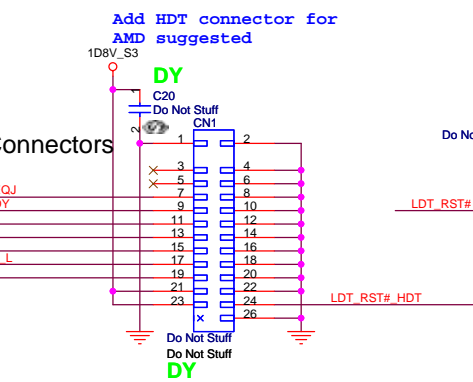
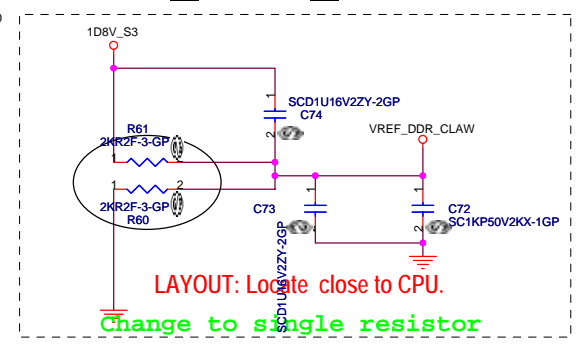


test

C36 near CLKCPU via



VREF_DDR_CLAW



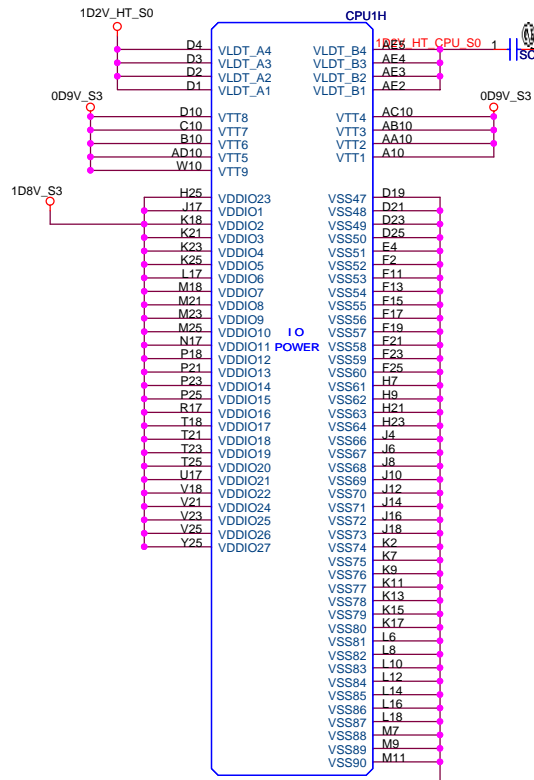
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

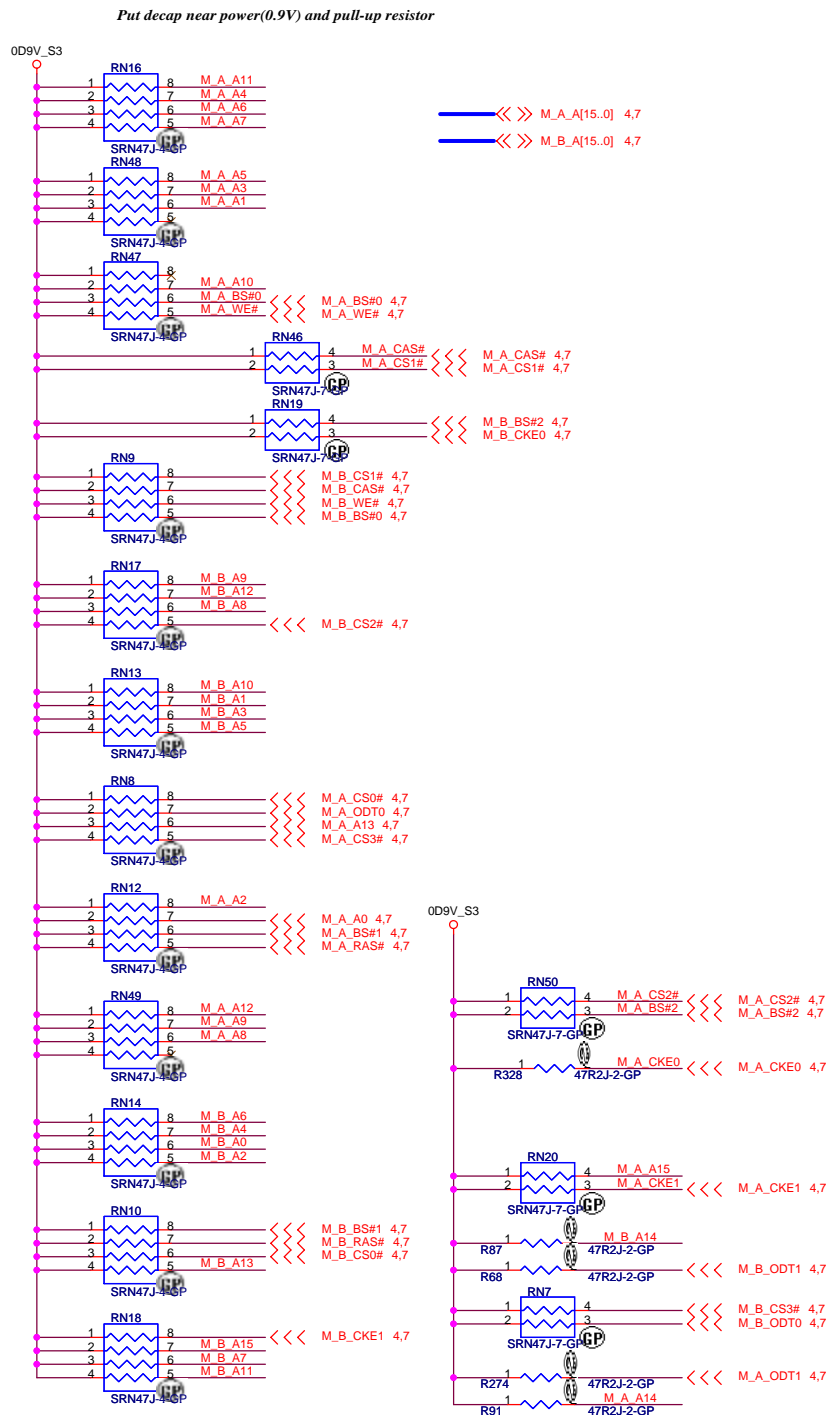
Title: **CPU(3/4) CONTROL**

Size A3 Document Number **TIBET** Rev **SA**

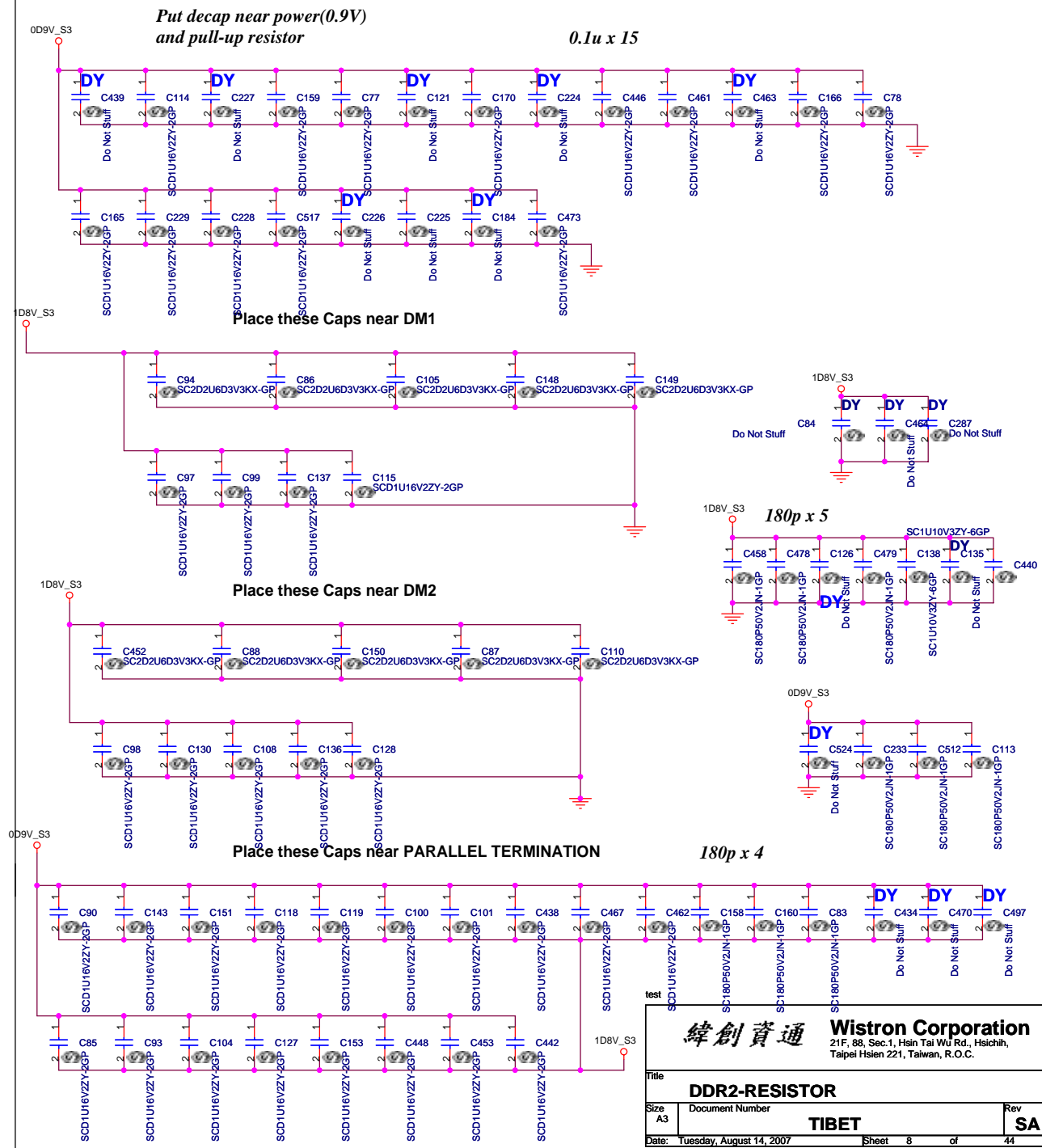
Date: Tuesday, August 14, 2007 Sheet 5 of 44



PARALLEL TERMINATION



Decoupling Capacitor



test

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Title	DDR2-RESISTOR	
Size	Document Number	Rev
A3		SA
Date: Tuesday, August 14, 2007	Sheet 8 of 44	

CPUCADOUT[15..0] 3
CPUCADOUTJ[15..0] 3

3 NB0CADOUT[15..0] 3
3 NB0CADOUTJ[15..0] 3

U55A 1 OF 8

HT

CPUCADOUT0	AF16	HT_MCP_RXD0_P
CPUCADOUTJ0	AG16	HT_MCP_RXD0_N
CPUCADOUT1	AH16	HT_MCP_RXD1_P
CPUCADOUTJ1	AJ16	HT_MCP_RXD1_N
CPUCADOUT2	AJ15	HT_MCP_RXD2_P
CPUCADOUTJ2	AK15	HT_MCP_RXD2_N
CPUCADOUT3	AK16	HT_MCP_RXD3_P
CPUCADOUTJ3	AL16	HT_MCP_RXD3_N
CPUCADOUT4	AG17	HT_MCP_RXD4_P
CPUCADOUTJ4	AF17	HT_MCP_RXD4_N
CPUCADOUT5	AL17	HT_MCP_RXD5_P
CPUCADOUTJ5	AK17	HT_MCP_RXD5_N
CPUCADOUT6	AL18	HT_MCP_RXD6_P
CPUCADOUTJ6	AK18	HT_MCP_RXD6_N
CPUCADOUT7	AJ19	HT_MCP_RXD7_P
CPUCADOUTJ7	AK19	HT_MCP_RXD7_N
CPUCADOUT8	AD14	HT_MCP_RXD8_P
CPUCADOUTJ8	AE14	HT_MCP_RXD8_N
CPUCADOUT9	AF14	HT_MCP_RXD9_P
CPUCADOUTJ9	AG14	HT_MCP_RXD9_N
CPUCADOUT10	AH14	HT_MCP_RXD10_P
CPUCADOUTJ10	AJ14	HT_MCP_RXD10_N
CPUCADOUT11	AL13	HT_MCP_RXD11_P
CPUCADOUTJ11	AK13	HT_MCP_RXD11_N
CPUCADOUT12	AC15	HT_MCP_RXD12_P
CPUCADOUTJ12	AD15	HT_MCP_RXD12_N
CPUCADOUT13	AD18	HT_MCP_RXD13_P
CPUCADOUTJ13	AE18	HT_MCP_RXD13_N
CPUCADOUT14	AE17	HT_MCP_RXD14_P
CPUCADOUTJ14	AD17	HT_MCP_RXD14_N
CPUCADOUT15	AB17	HT_MCP_RXD15_P
CPUCADOUTJ15	AC17	HT_MCP_RXD15_N

HT_MCP_TXD0_P	AK27	NB0CADOUT0
HT_MCP_TXD0_N	AJ27	NB0CADOUTJ0
HT_MCP_TXD1_P	AK26	NB0CADOUT1
HT_MCP_TXD1_N	AL26	NB0CADOUTJ1
HT_MCP_TXD2_P	AK25	NB0CADOUT2
HT_MCP_TXD2_N	AL25	NB0CADOUTJ2
HT_MCP_TXD3_P	AK24	NB0CADOUT3
HT_MCP_TXD3_N	AK22	NB0CADOUT4
HT_MCP_TXD4_P	AL22	NB0CADOUTJ4
HT_MCP_TXD5_P	AK21	NB0CADOUT5
HT_MCP_TXD5_N	AL21	NB0CADOUTJ5
HT_MCP_TXD6_P	AJ21	NB0CADOUT6
HT_MCP_TXD6_N	AL20	NB0CADOUT7
HT_MCP_TXD7_P	AM20	NB0CADOUTJ7
HT_MCP_TXD8_P	AG27	NB0CADOUT8
HT_MCP_TXD8_N	AH27	NB0CADOUTJ8
HT_MCP_TXD9_P	AE25	NB0CADOUT9
HT_MCP_TXD9_N	AG25	NB0CADOUTJ9
HT_MCP_TXD10_P	AH25	NB0CADOUT10
HT_MCP_TXD10_N	AJ25	NB0CADOUTJ10
HT_MCP_TXD11_P	AE23	NB0CADOUT11
HT_MCP_TXD11_N	AE23	NB0CADOUTJ11
HT_MCP_TXD12_P	AD21	NB0CADOUT12
HT_MCP_TXD12_N	AE21	NB0CADOUTJ12
HT_MCP_TXD13_P	AE21	NB0CADOUT13
HT_MCP_TXD13_N	AG21	NB0CADOUTJ13
HT_MCP_TXD14_P	AC20	NB0CADOUT14
HT_MCP_TXD14_N	AD20	NB0CADOUTJ14
HT_MCP_TXD15_P	AE19	NB0CADOUT15
HT_MCP_TXD15_N	AE19	NB0CADOUTJ15

3 CPUHTTCLKOUT0	>>>	CPUHTTCLKOUT0	AJ17	HT_MCP_RX_CLK0_P
3 CPUHTTCLKOUTJ0	>>>	CPUHTTCLKOUTJ0	AH17	HT_MCP_RX_CLK0_N
3 CPUHTTCLKOUT1	>>>	CPUHTTCLKOUT1	AL14	HT_MCP_RX_CLK1_P
3 CPUHTTCLKOUTJ1	>>>	CPUHTTCLKOUTJ1	AK14	HT_MCP_RX_CLK1_N

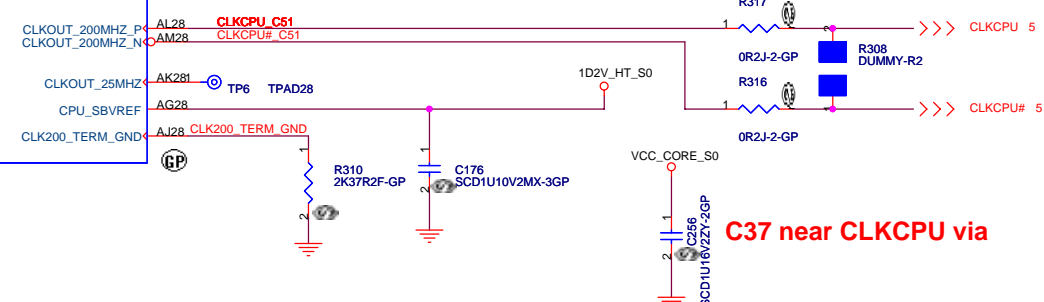
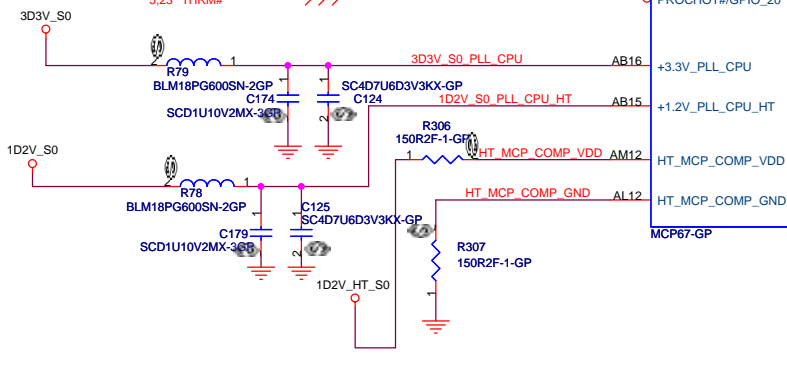
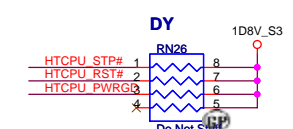
HT_MCP_TX_CLK0_P	AK23	NB0HTTCLKOUT0	>>>	NB0HTTCLKOUT0 3
HT_MCP_TX_CLK0_N	AJ23	NB0HTTCLKOUTJ0	>>>	NB0HTTCLKOUTJ0 3
HT_MCP_TX_CLK1_P	AG23	NB0HTTCLKOUT1	>>>	NB0HTTCLKOUT1 3
HT_MCP_TX_CLK1_N	AH23	NB0HTTCLKOUTJ1	>>>	NB0HTTCLKOUTJ1 3

3 CPUHTTCTLOUT0	>>>	CPUHTTCTLOUT0	AH19	HT_MCP_RXCTL0_P
3 CPUHTTCTLOUTJ0	>>>	CPUHTTCTLOUTJ0	AG19	HT_MCP_RXCTL0_N
			AC18	RESERVED#AC18
			AD18	RESERVED#AD18

HT_MCP_TXCTL0_P	AK20	NB0HTTCTLOUT 3	>>>	NB0HTTCTLOUT 3
HT_MCP_TXCTL0_N	AJ20	NB0HTTCTLOUTJ 3	>>>	NB0HTTCTLOUTJ 3
RESERVED#AD19	AD19			
RESERVED#AC19	AC19			

5 CPU_THERMTRIP# >>> AC13 THERMTRIP#/GPIO_58
5.23 THR# >>> AB13 PROCHOT#/GPIO_20

HT_MCP_REQ#	AD23	HT_CPU_REQ#	1	
HT_MCP_STOP#	AB20			
HT_MCP_RST#	AC21			
HT_MCP_PWRGD	AD22			

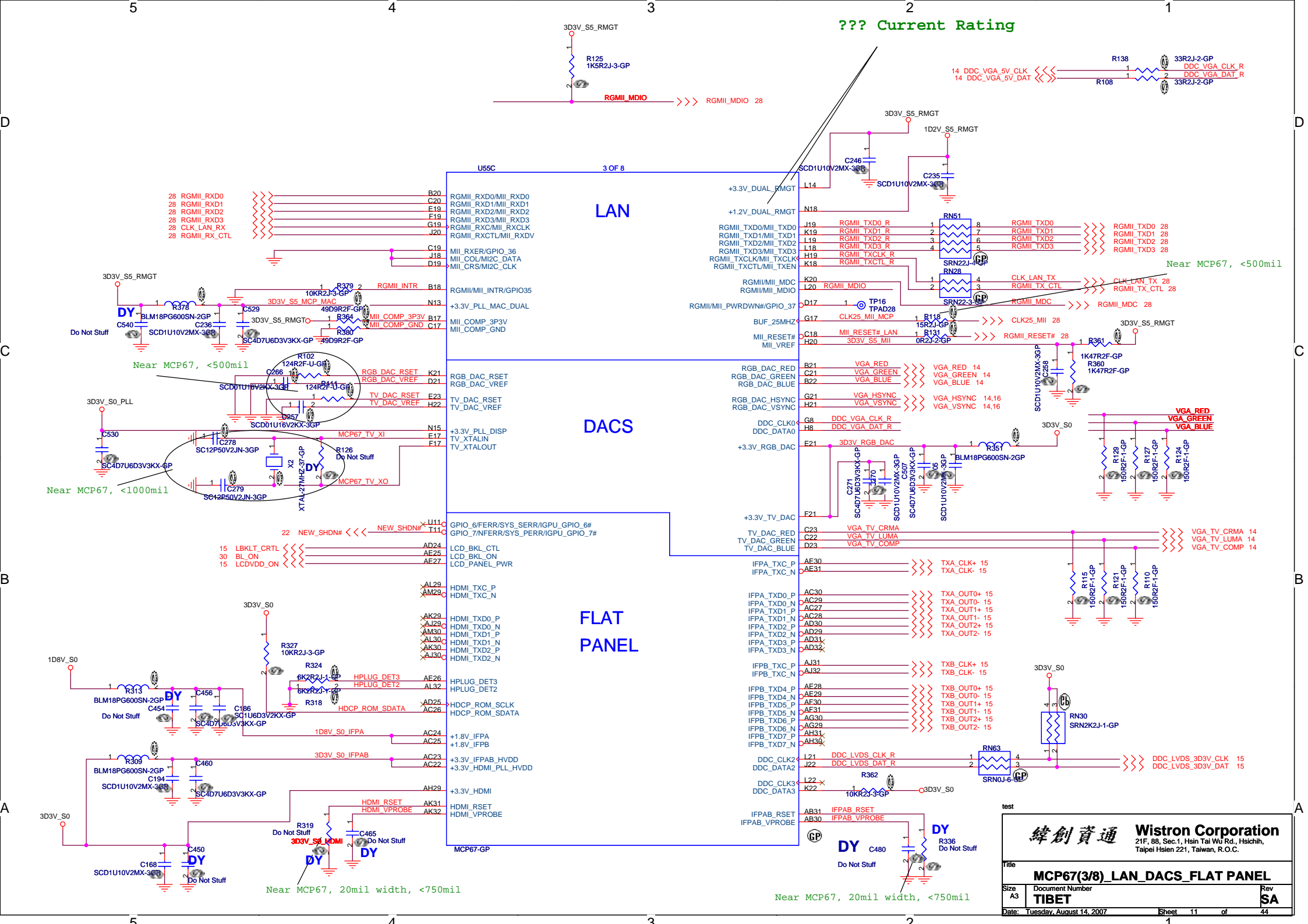


test

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP67(1/8) HT CPU**

Size: A3	Document Number: TIBET	Rev: SA
Date: Tuesday, August 14, 2007	Sheet: 9	of: 44



??? Current Rating

LAN

DACS

FLAT PANEL

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP67(3/8)_LAN_DACS_FLAT_PANEL**

Size: A3 Document Number: **TIBET** Rev: SA

Date: Tuesday, August 14, 2007 Sheet 11 of 44

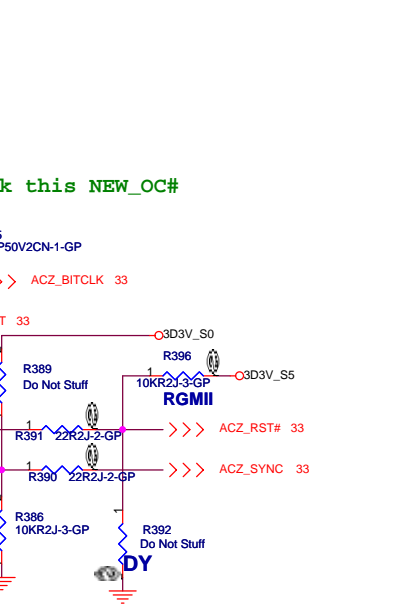
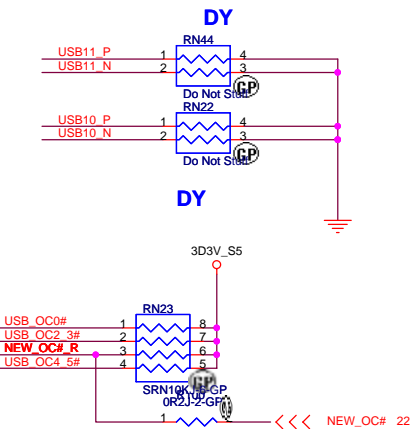
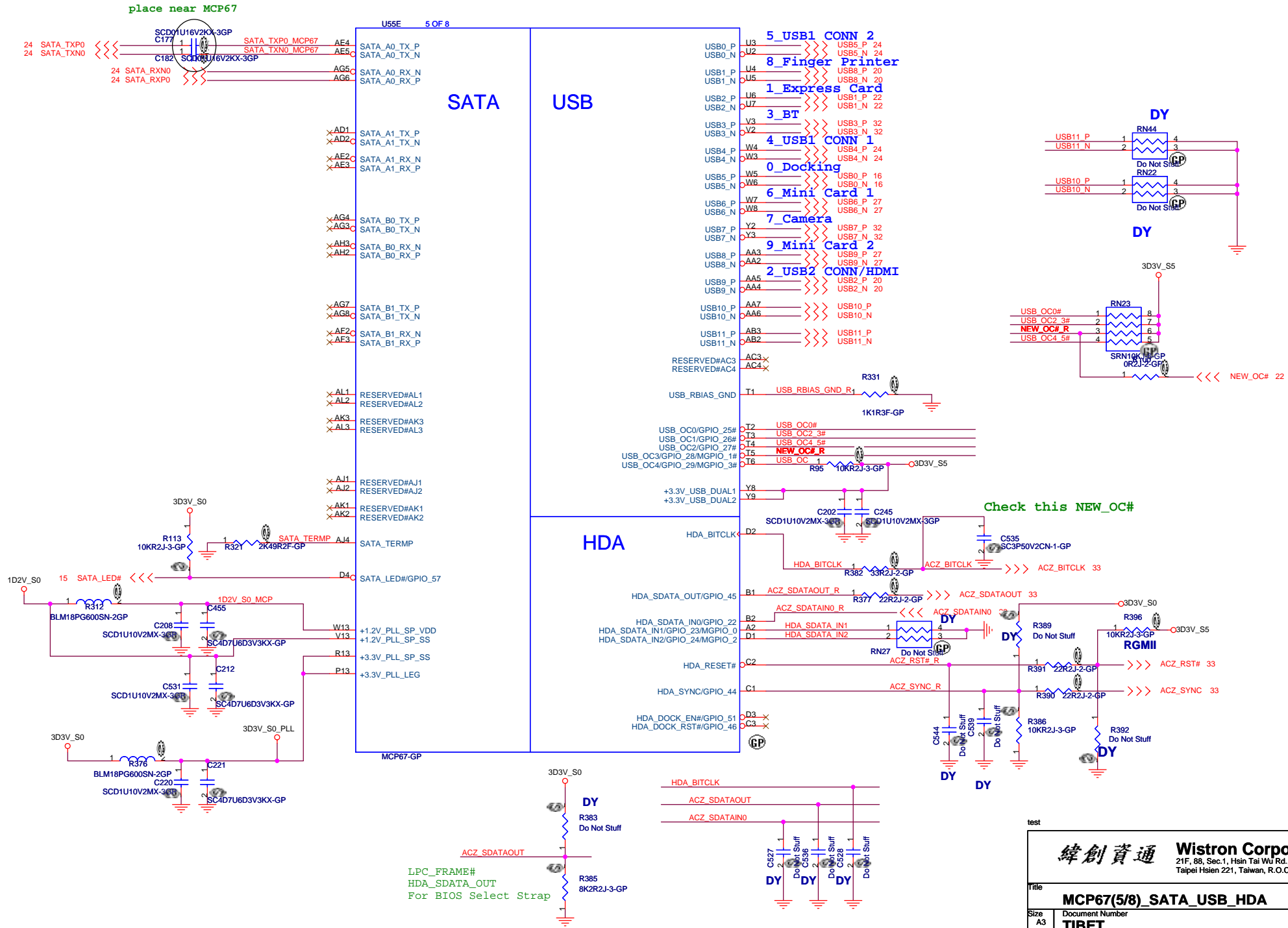
Near MCP67, 20mil width, <750mil

Near MCP67, 20mil width, <750mil

Near MCP67, <500mil

Near MCP67, <1000mil

Near MCP67, <500mil



test

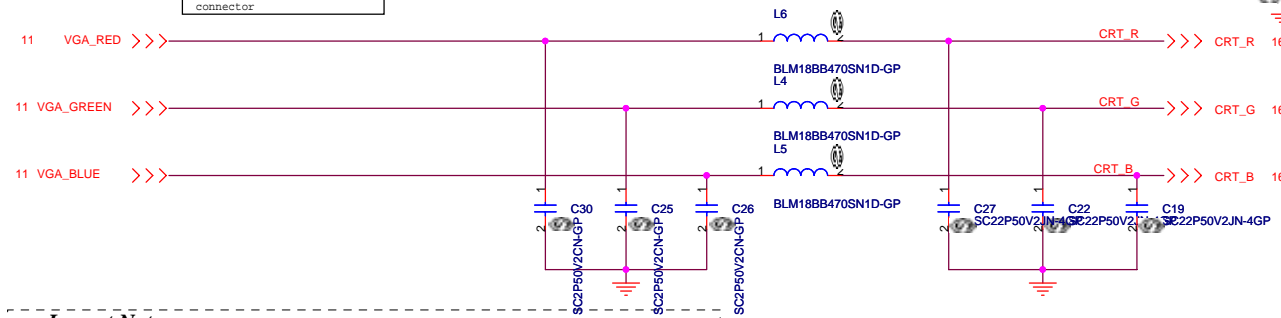
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP67(5/8)_SATA_USB_HDA**

Size: A3	Document Number: TIBET	Rev: SA
Date: Tuesday, August 14, 2007	Sheet: 13	of: 44

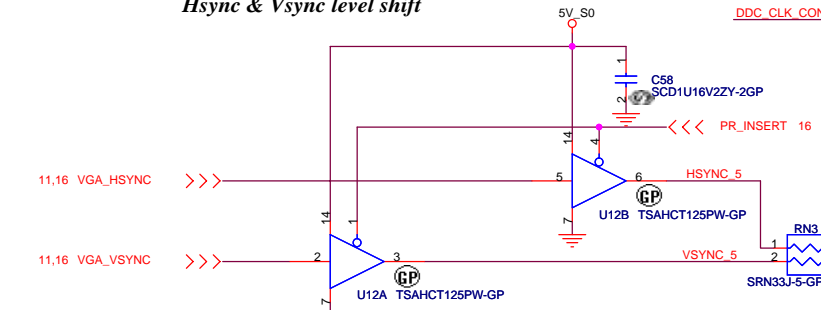
CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector



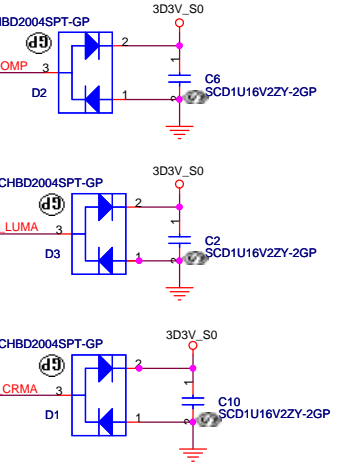
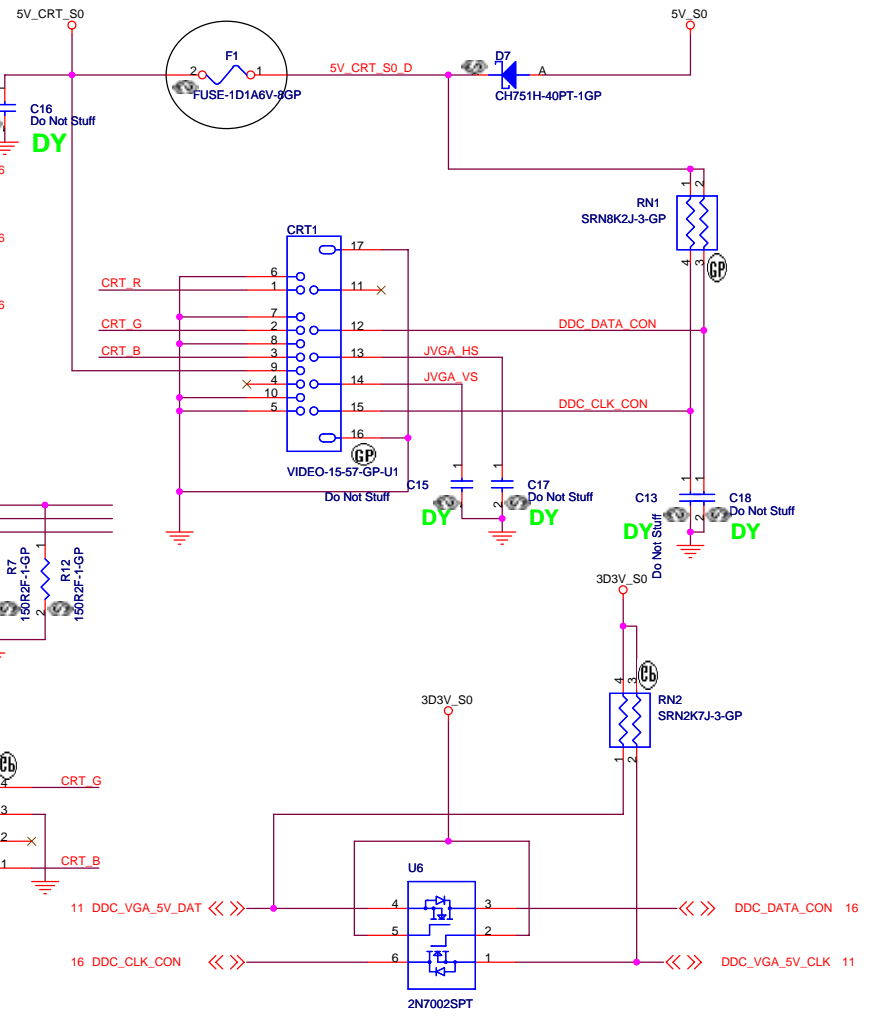
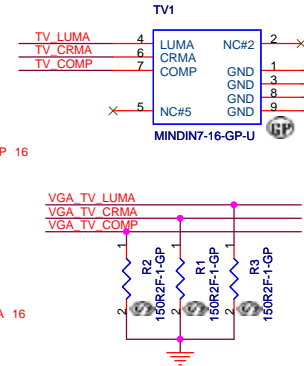
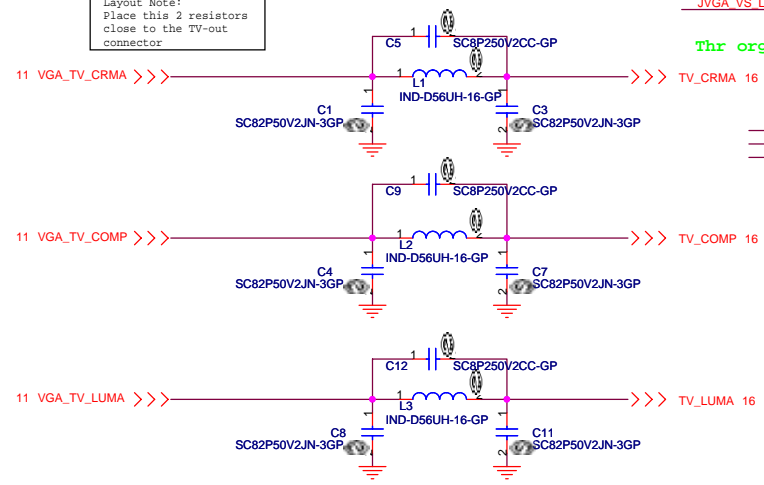
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift



TV OUT CONN

Layout Note:
Place this 2 resistors
close to the TV-out
connector



5V @ ext. CRT side

test

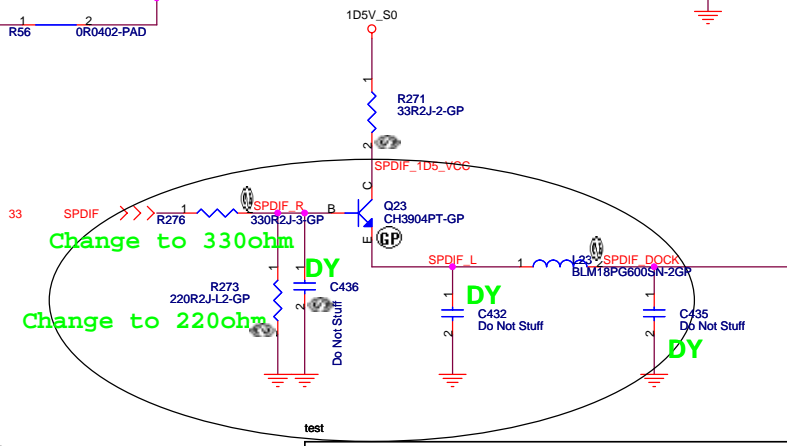
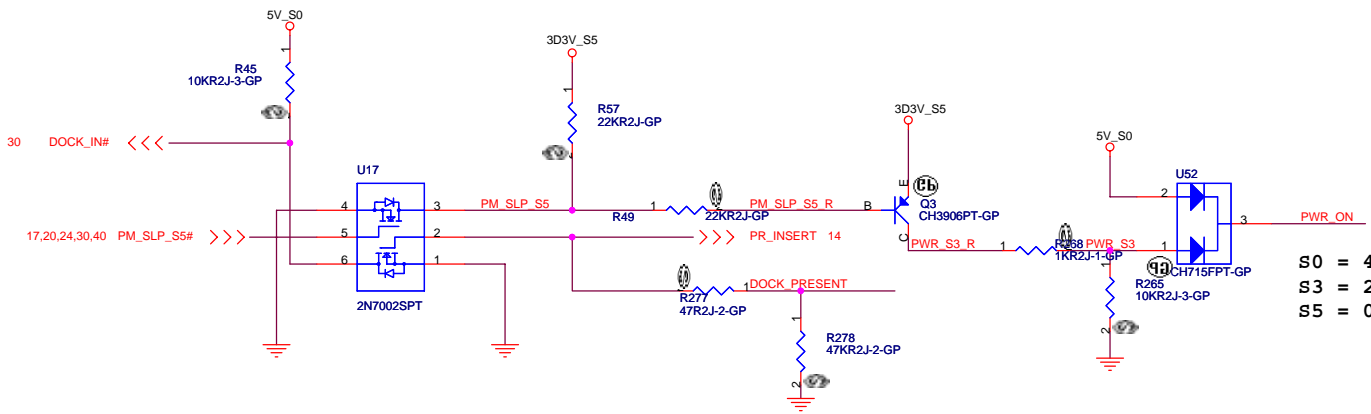
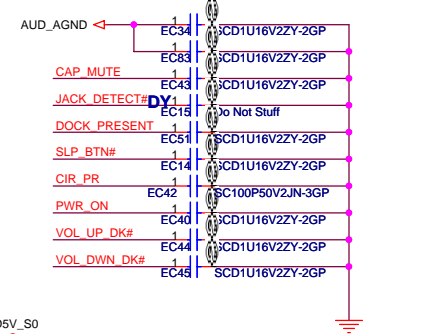
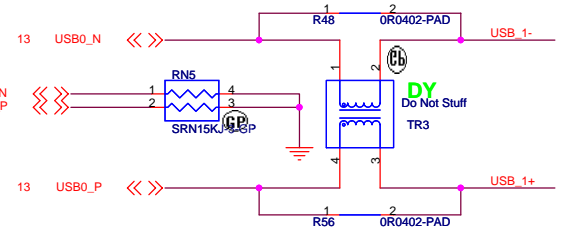
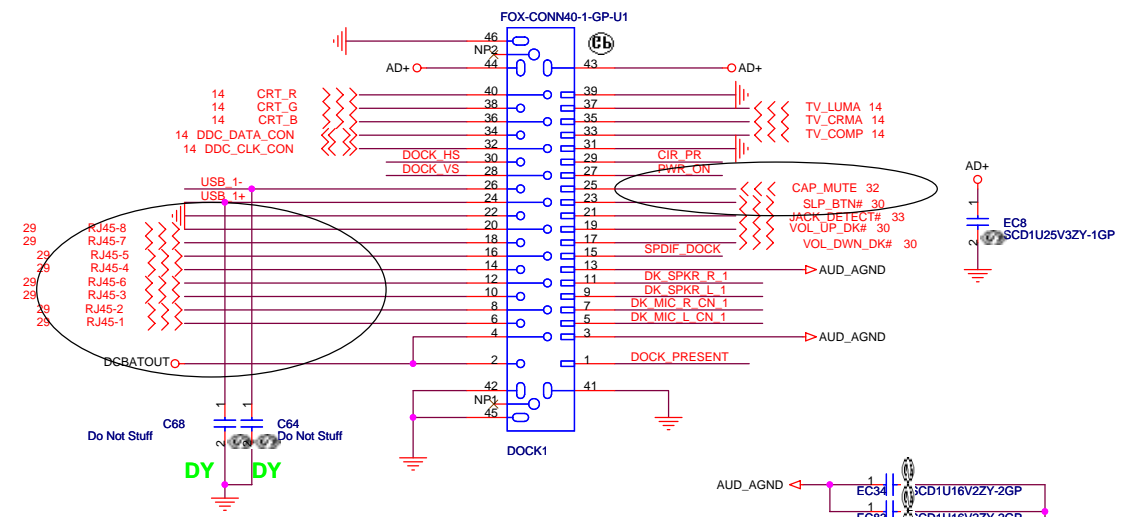
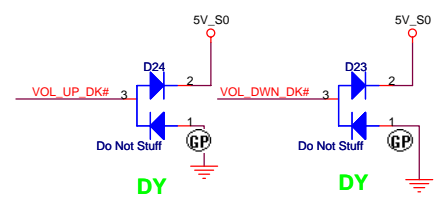
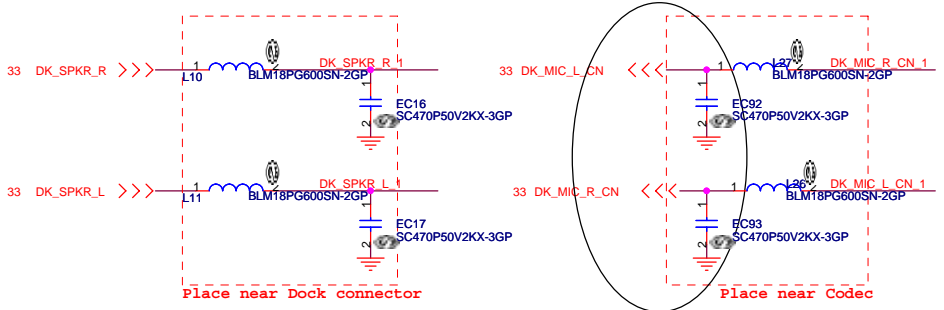
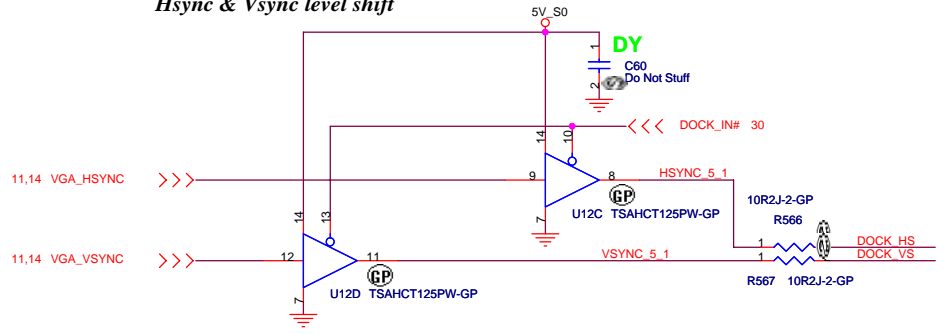
緯創資通 Wistron Corporation
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Title: **CRT/TV CONNECTOR**

Size A3	Document Number	Rev
	TIBET	SA
Date: Tuesday, August 14, 2007	Sheet 14 of 44	

Docking Connector

Hsync & Vsync level shift

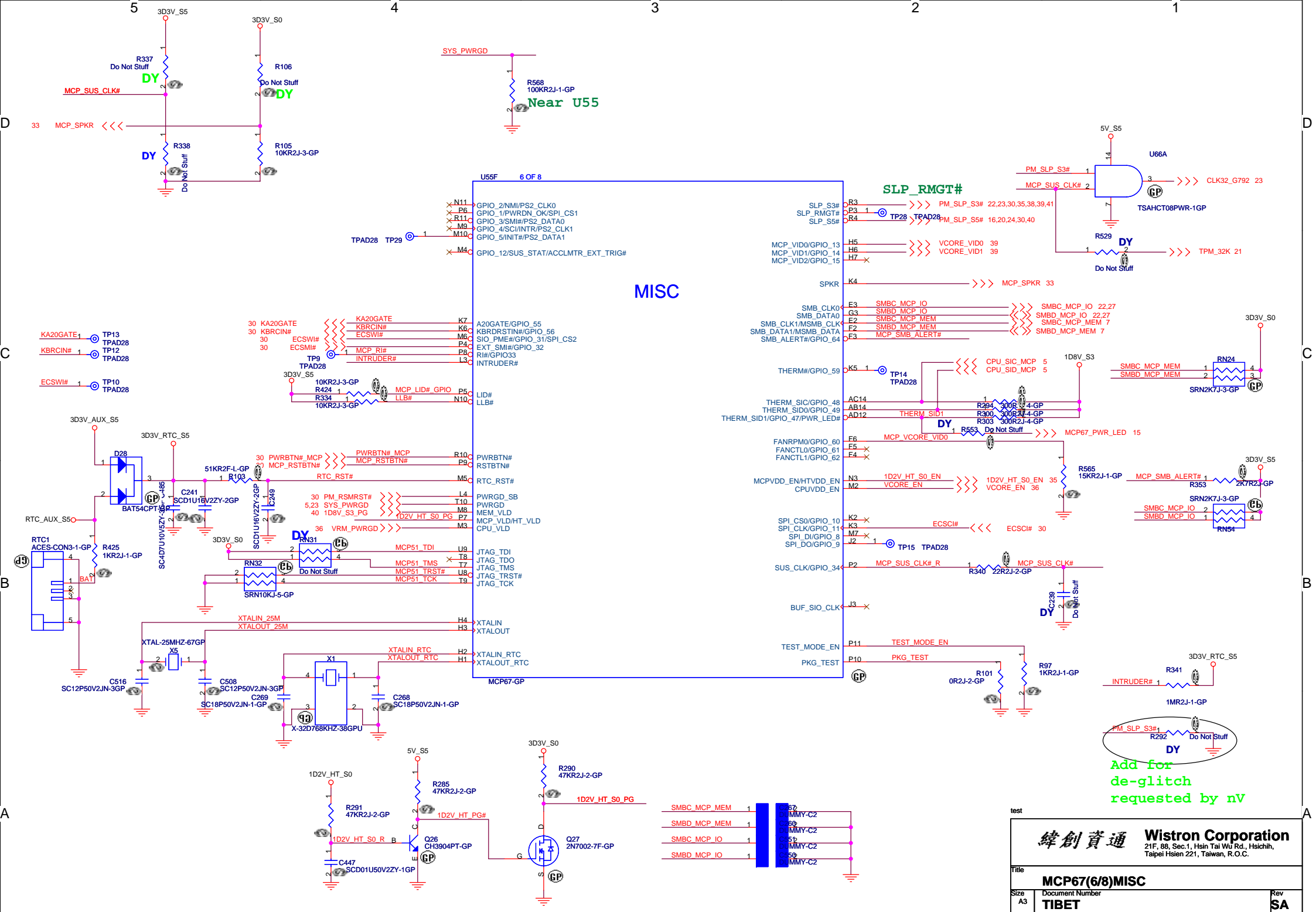


S0 = 4V
S3 = 2.5V
S5 = 0V

緯創資通 Wistron Corporation
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Title: **Board to board conn/ Docking**

Size A3	Document Number	Rev SA
TIBET		
Date: Tuesday, August 14, 2007	Sheet 16	of 44



test

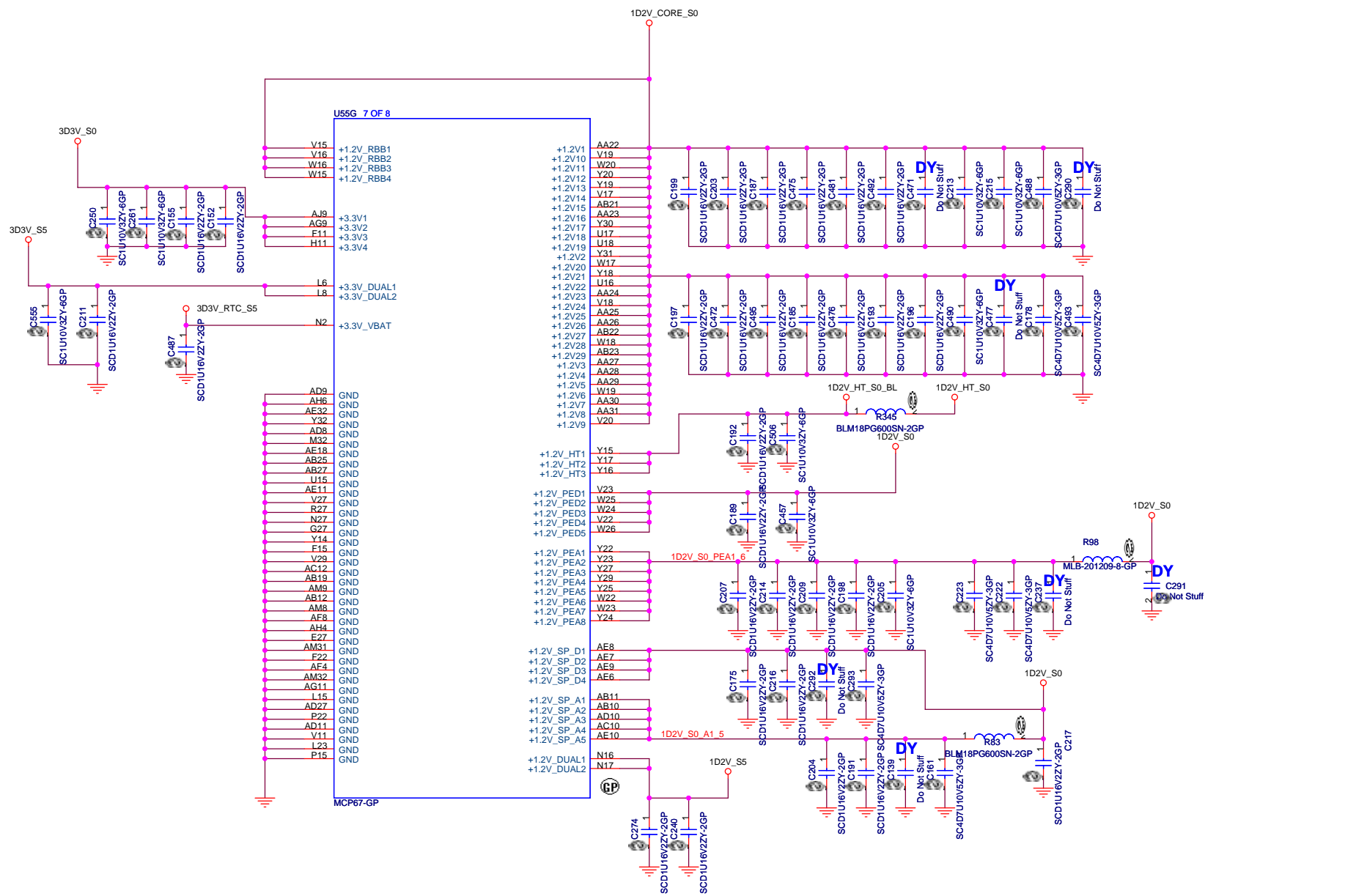
緯創資通 Wistron Corporation
 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP67(6/8)MISC**

Size: A3
 Document Number: **TIBET**

Date: Tuesday, August 14, 2007
 Sheet 17 of 44

Rev SA



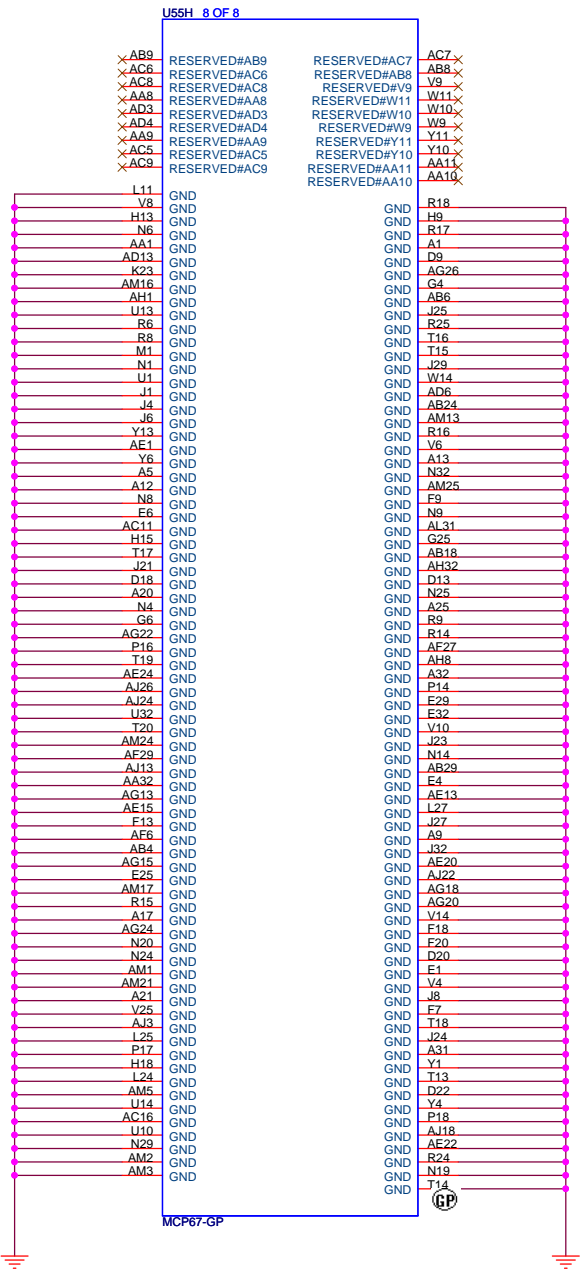
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP67(7/8)_POWER**

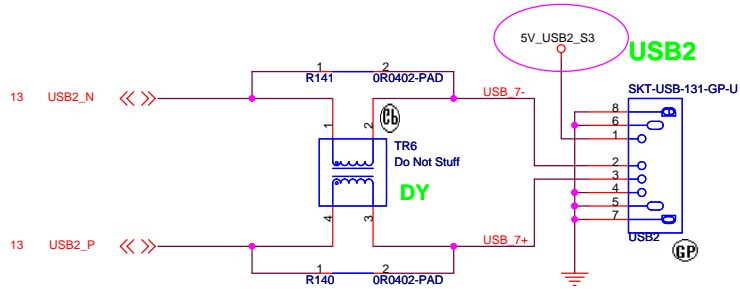
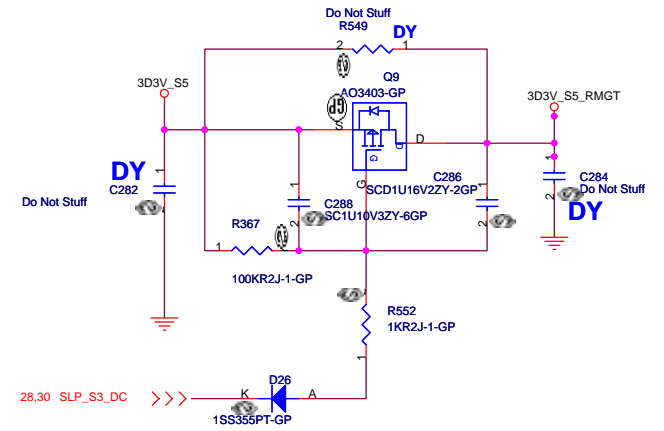
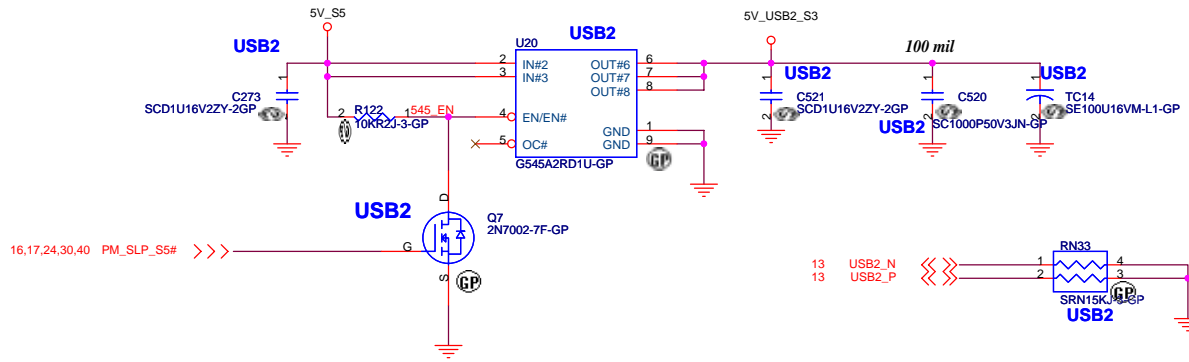
Size: A3 Document Number: **TIBET** Rev: **SA**

Date: Tuesday, August 14, 2007 Sheet 18 of 44

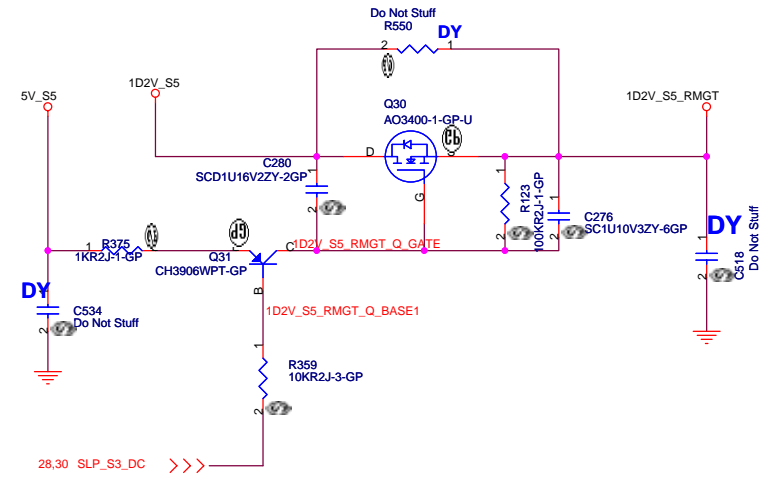


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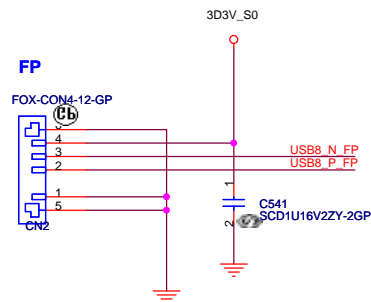
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MCP67(8/8)_GND			
Size	Document Number	Date:	Rev
A3	TIBET	Tuesday, August 14, 2007	SA
		Sheet 19 of 44	



??? Current Rating



Finger Printer

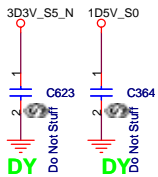


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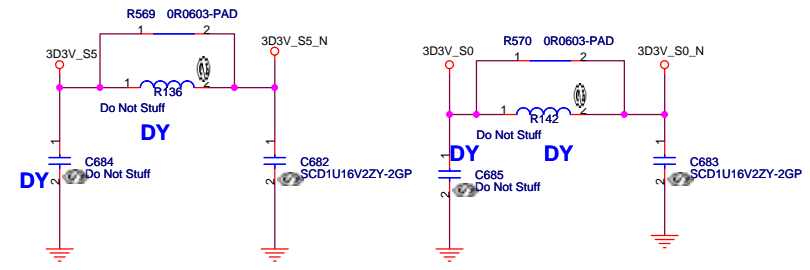
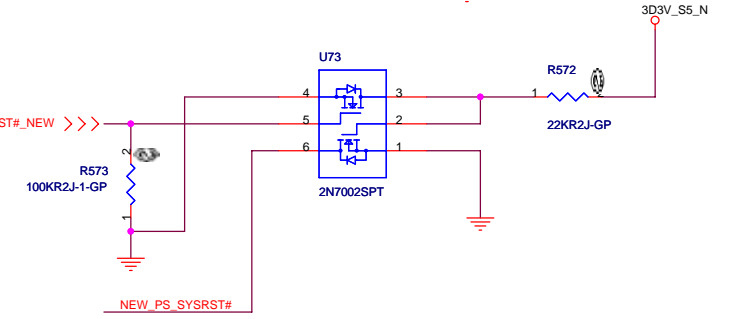
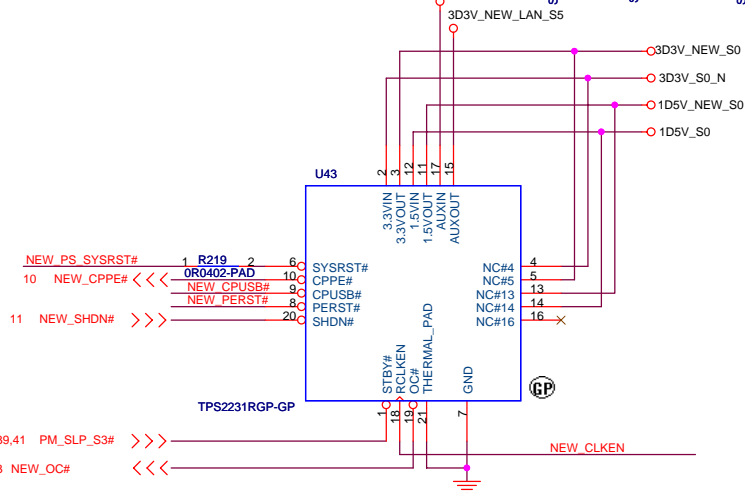
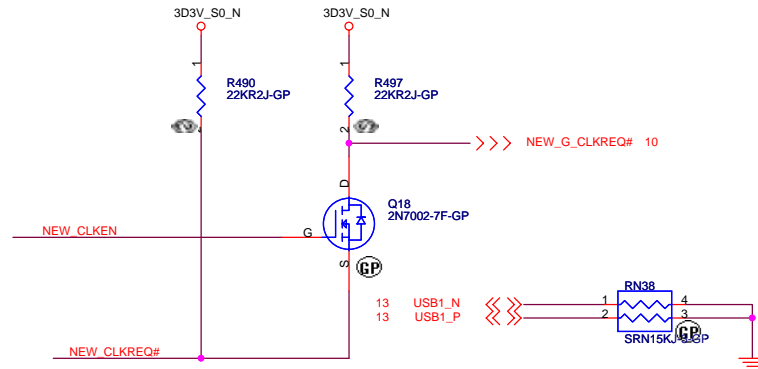
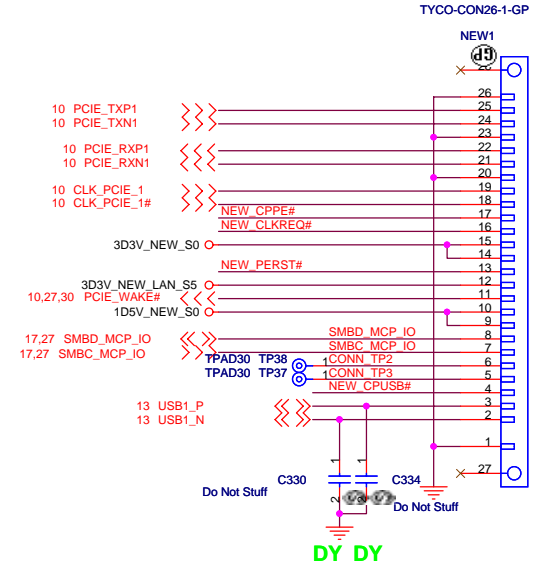
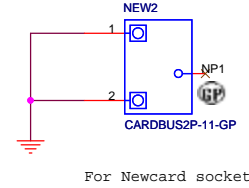
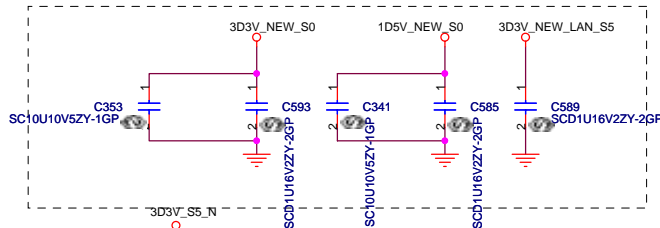
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDMI/FINGER PRINTER			
Size	Document Number		Rev
A3	TIBET		SA
Date: Tuesday, August 14, 2007		Sheet 20	of 44

NEWCARD Connector

Place them Near to Chip



Place them Near to Connector



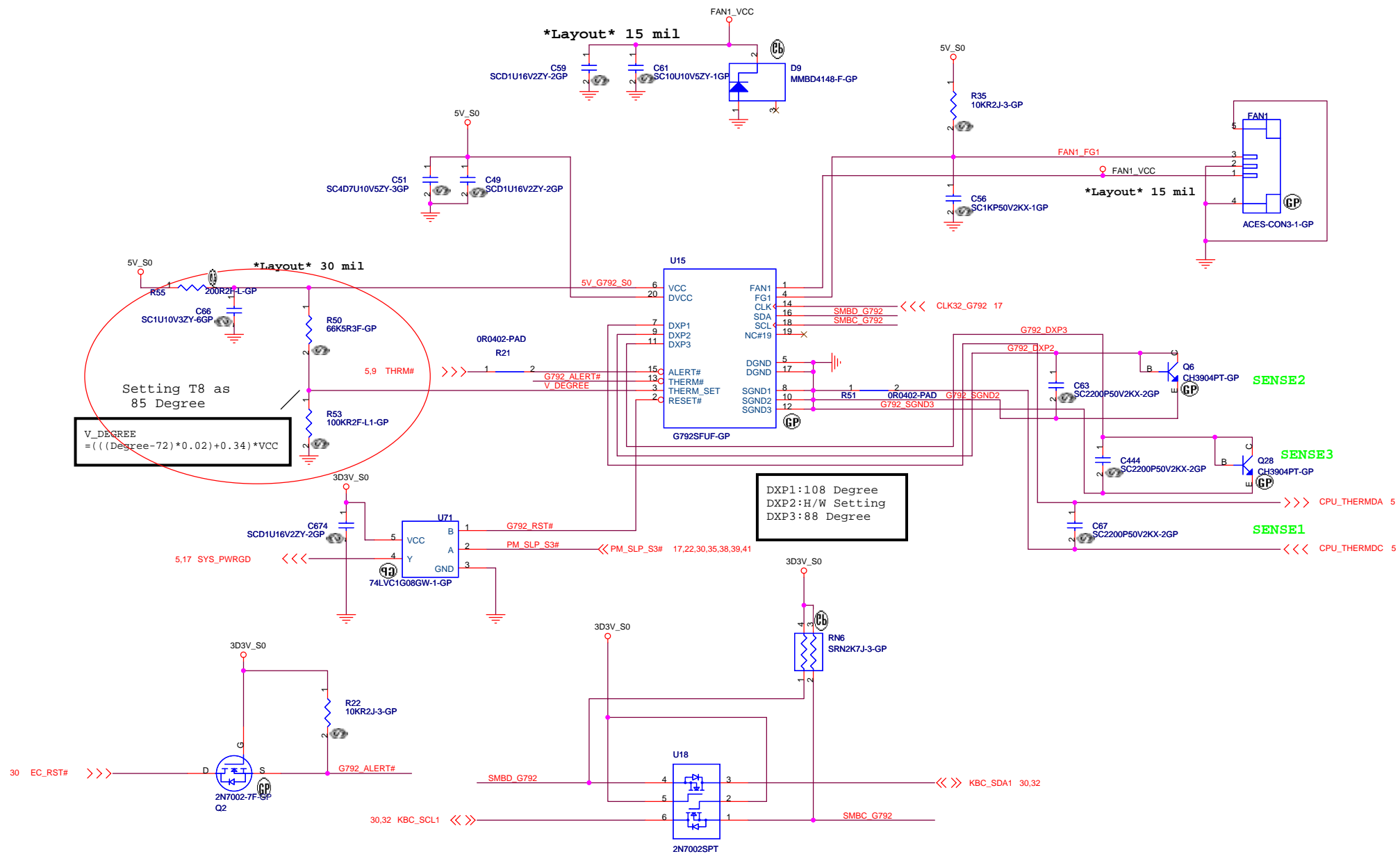
test

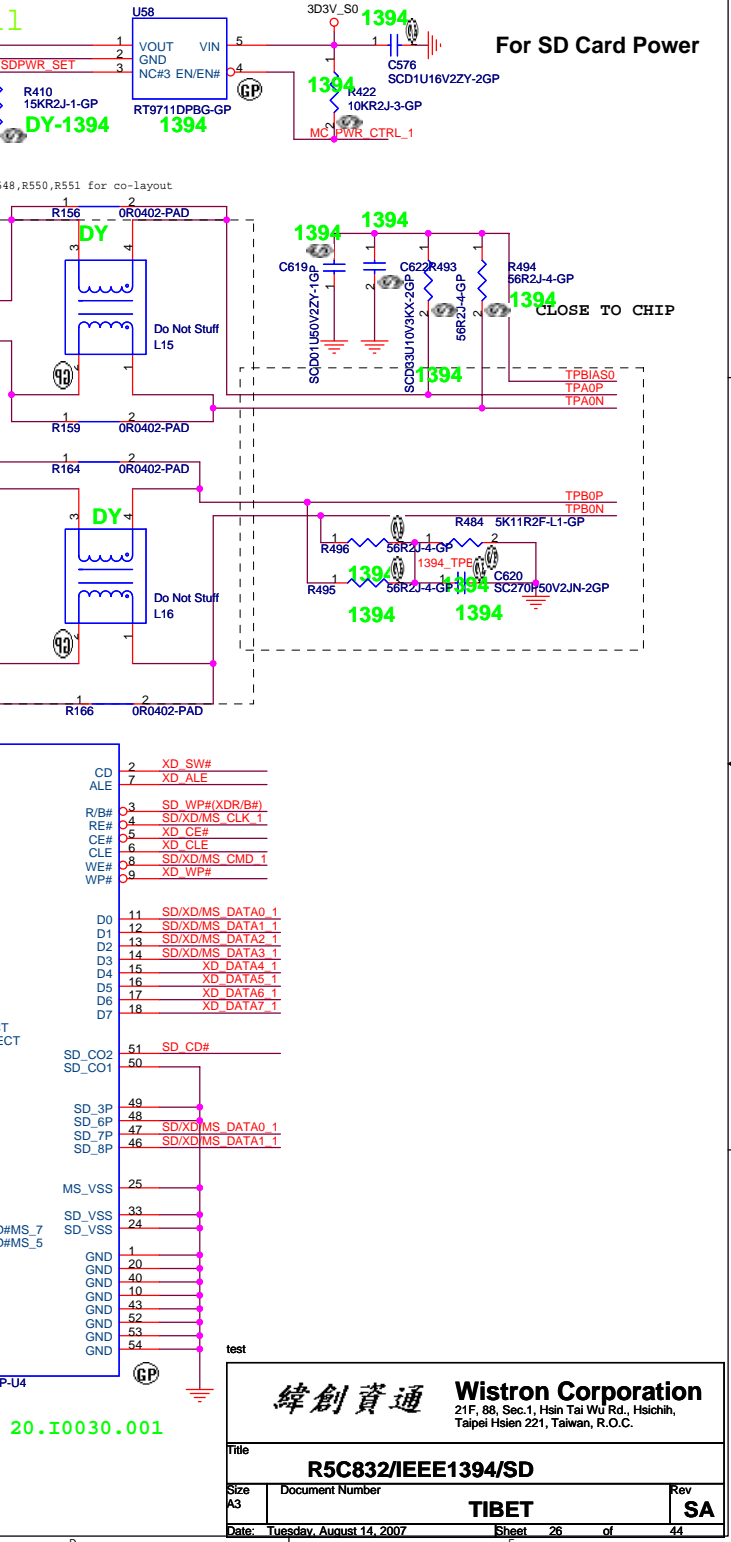
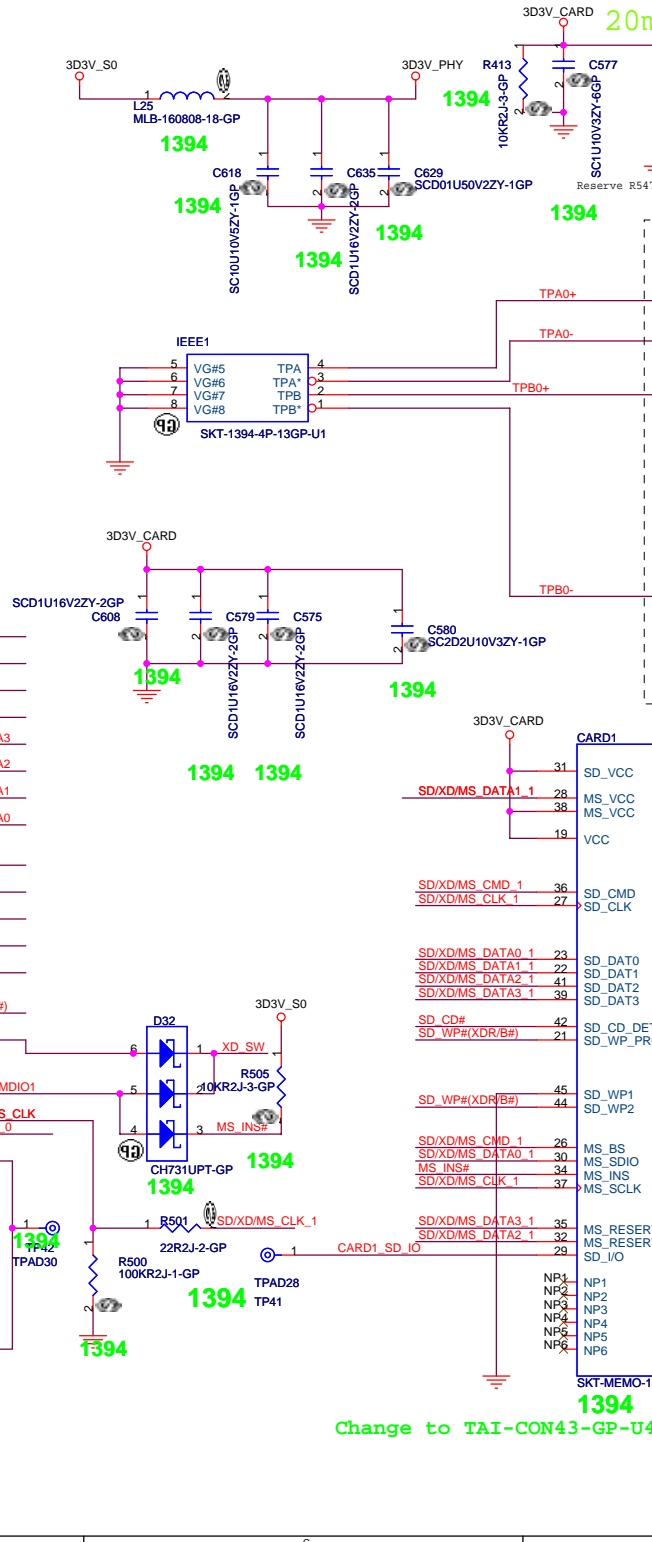
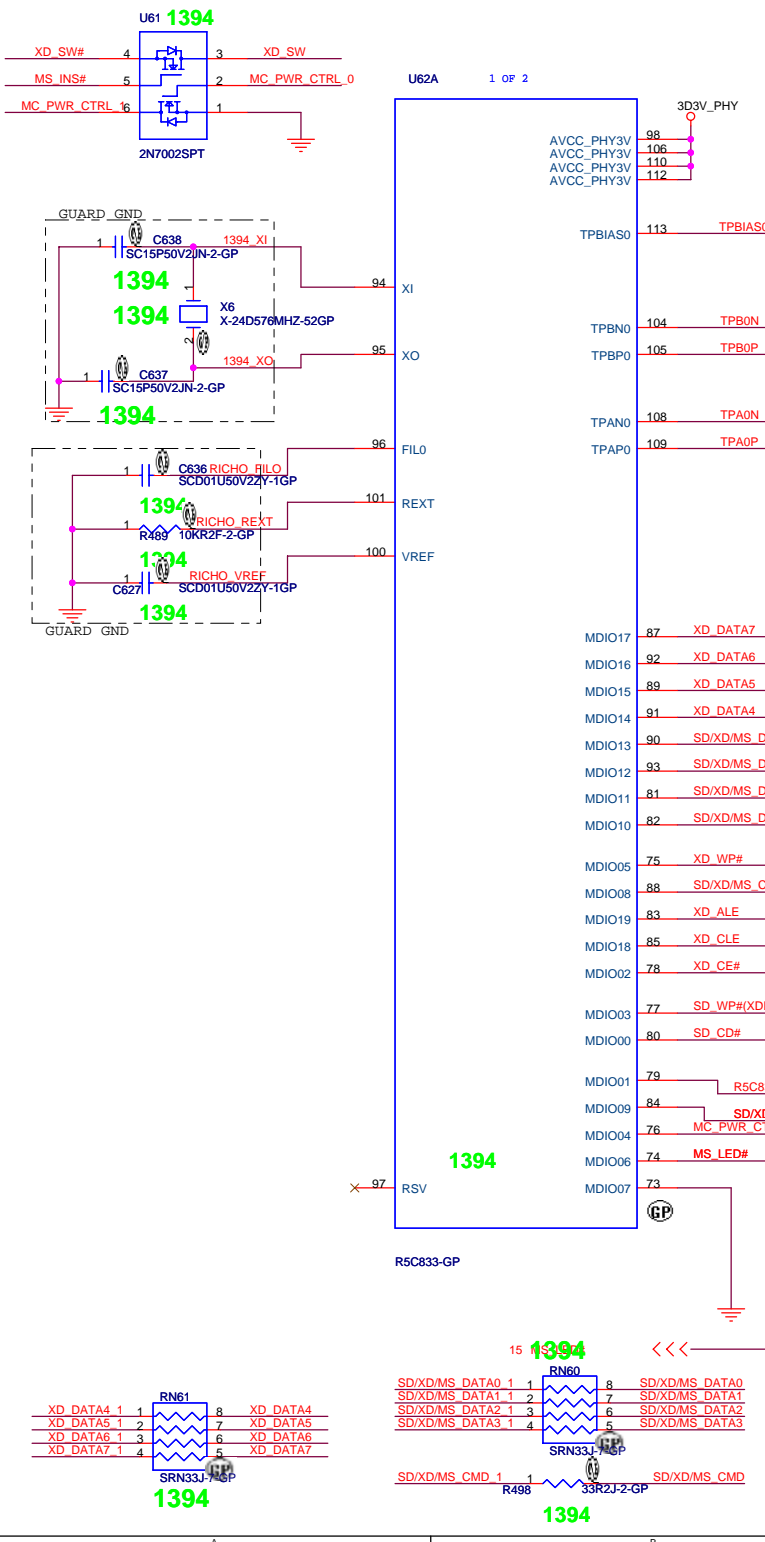
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **NEW CARD**

Size: A3 | Document Number: **TIBET** | Rev: **SA**

Date: Tuesday, August 14, 2007 | Sheet: 22 of 44





Change to TAI-CON43-GP-U4, 20.I0030.001

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **R5C832/IEEE1394/SD**

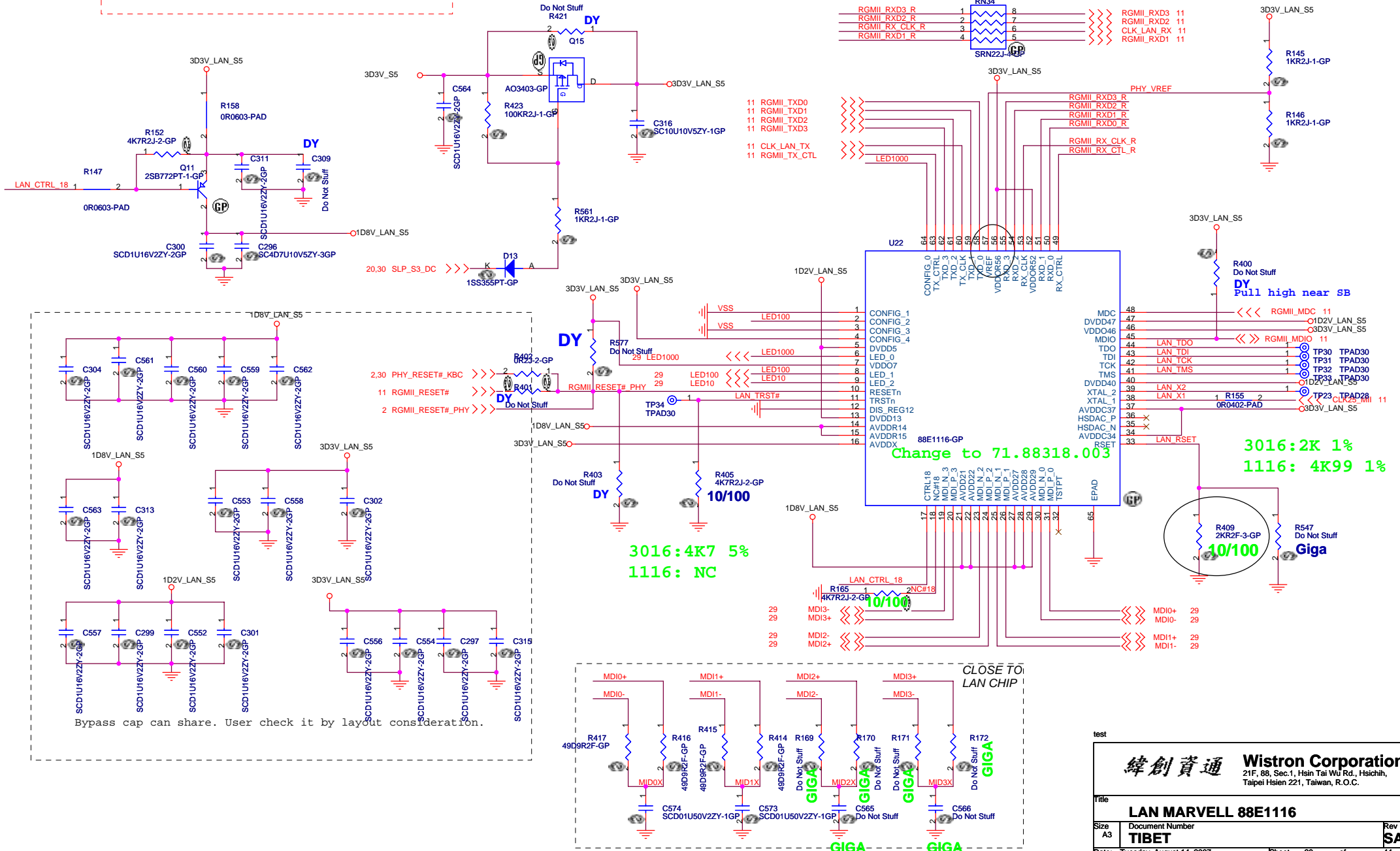
Size: A3
Date: Tuesday, August 14, 2007

Document Number: **TIBET**
Sheet: 26 of 44

Rev: SA

1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities

E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.

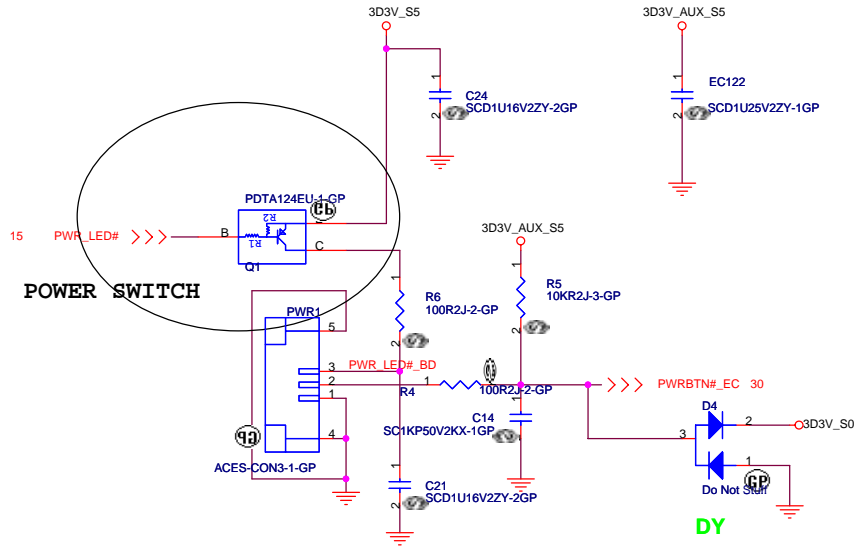


GOLDEN FINGER FOR DEBUG BOARD

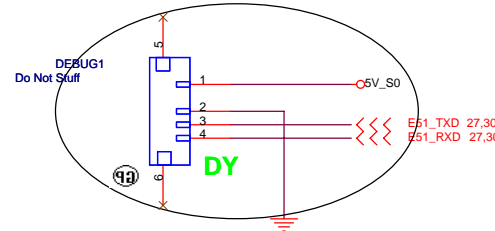
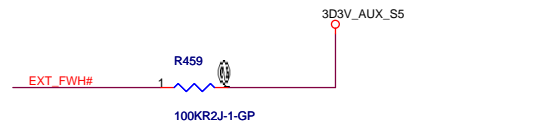
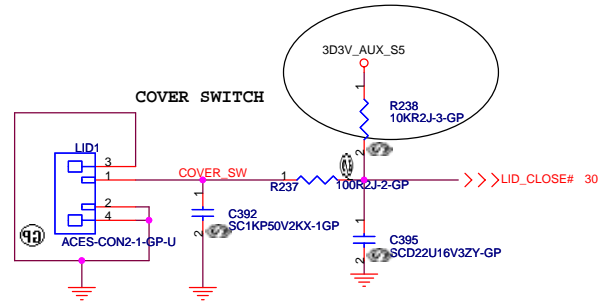
TOP VIEW

A15 (B1)
A14 (B2)
⋮
A2 (B14)
A1 (B15)

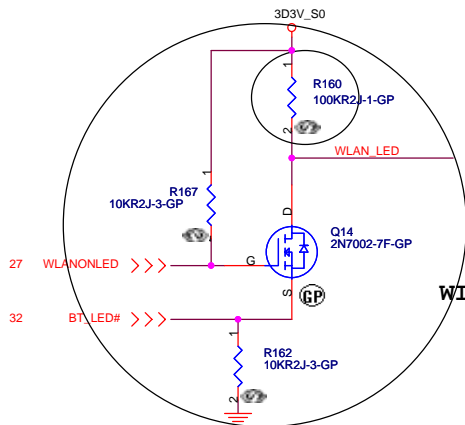
(BOTTOM VIEW)



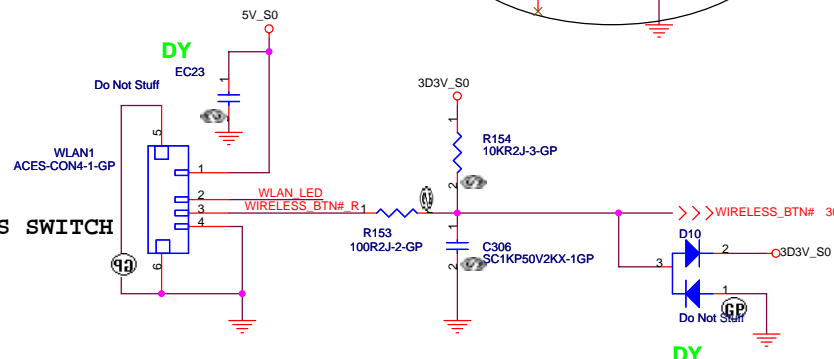
DY



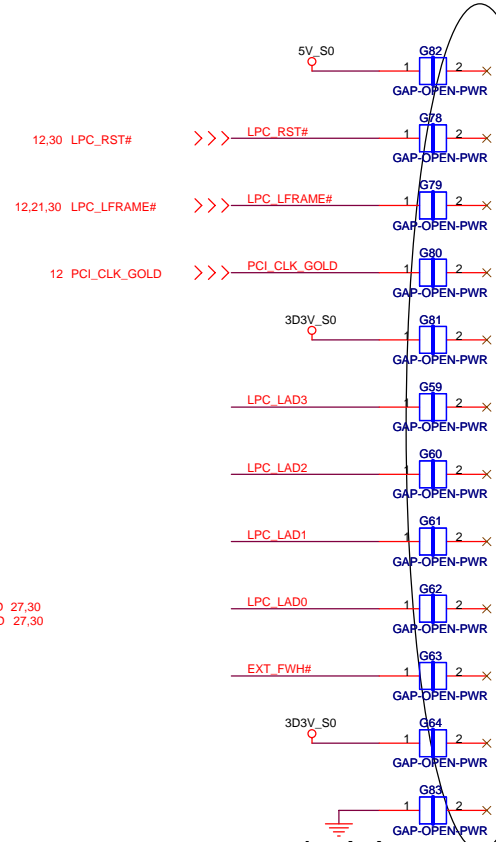
DY



WIRELESS SWITCH

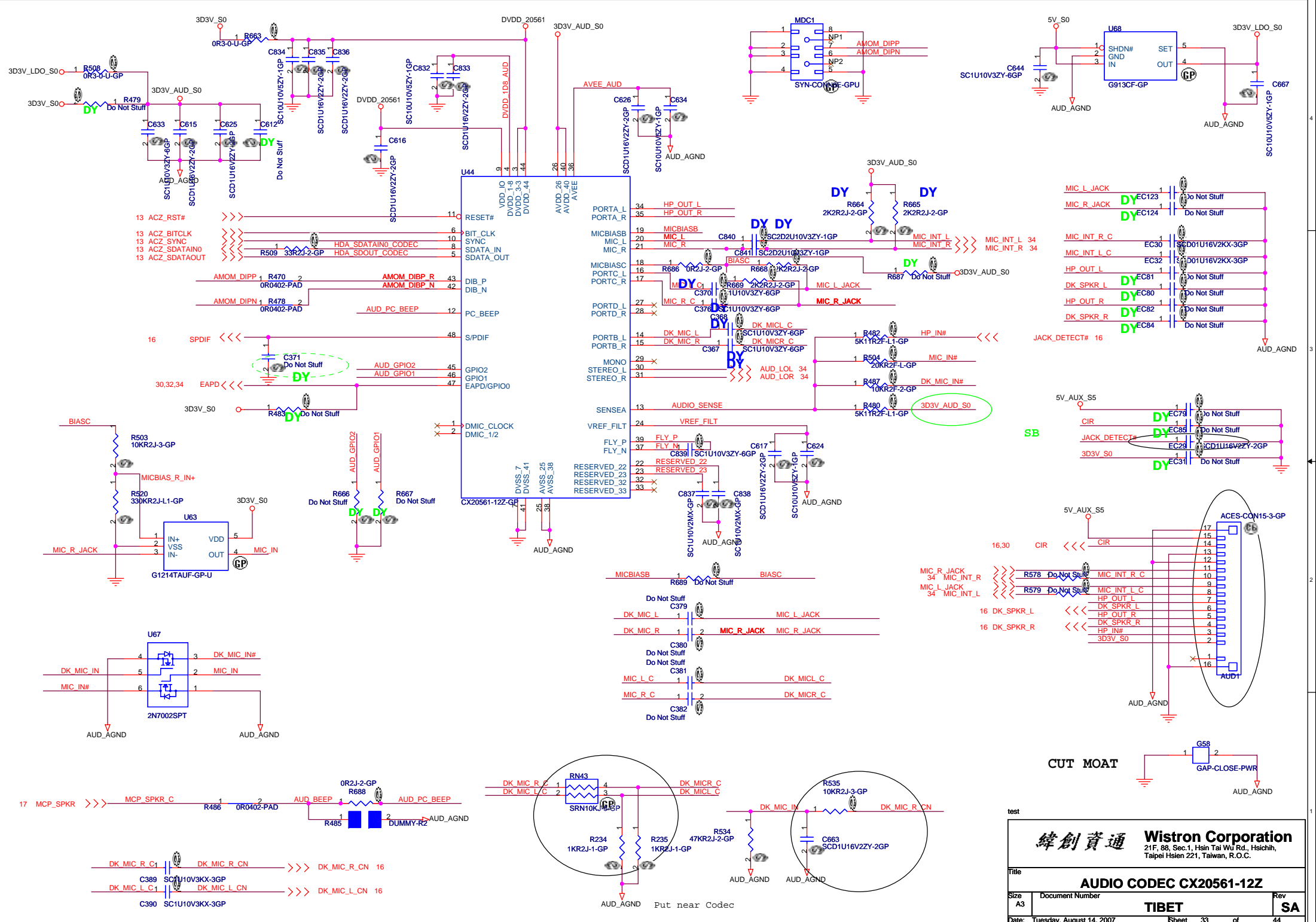


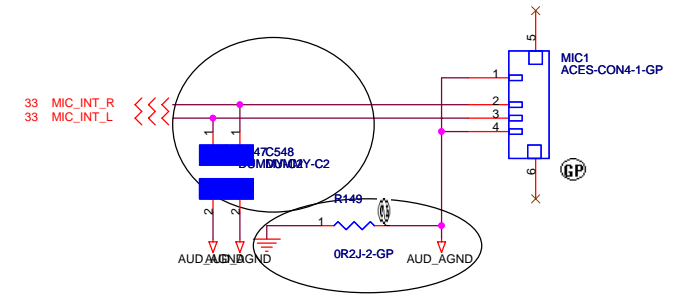
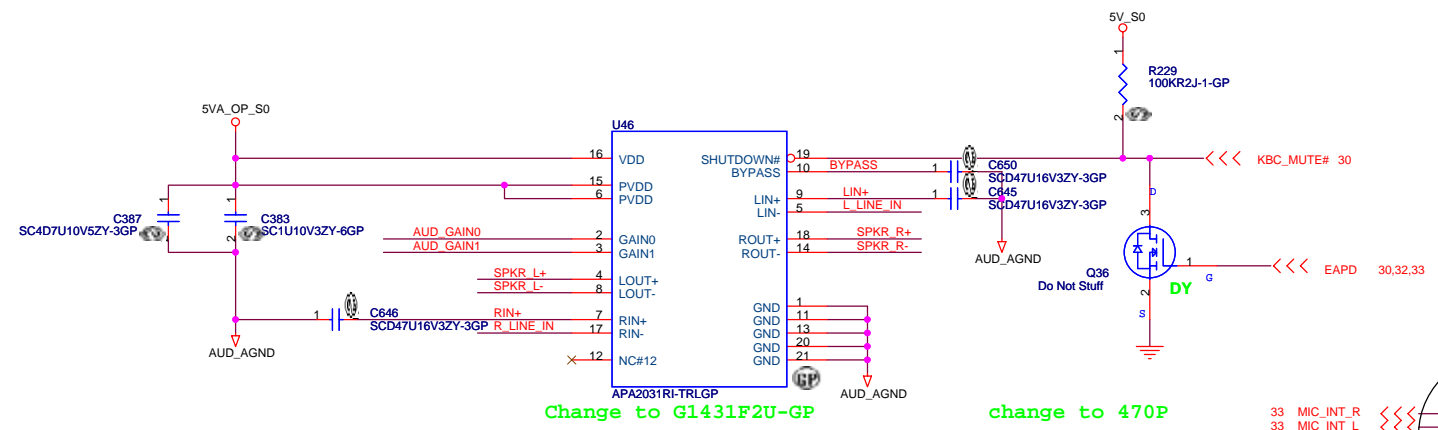
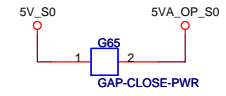
DY



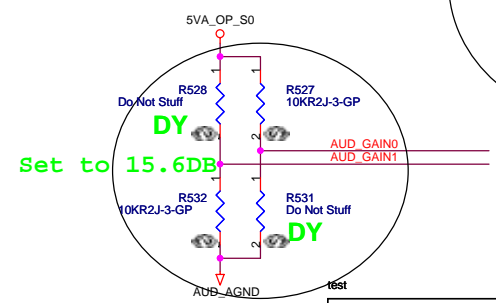
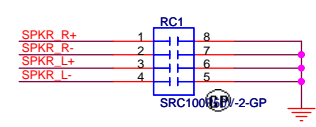
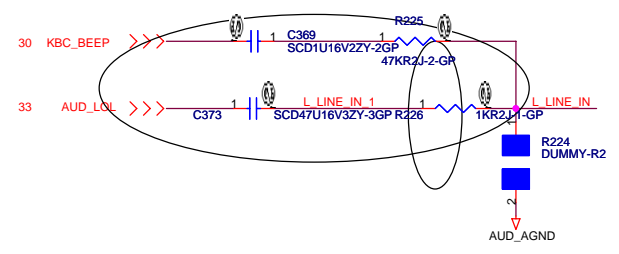
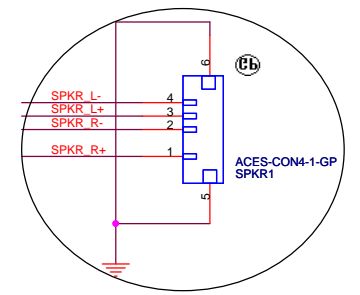
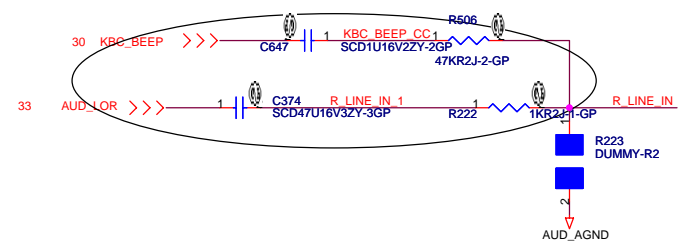
Put near board edge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
FLASH and Debug		
Size	Document Number	Rev
A3		SA
Date: Tuesday, August 14, 2007		Sheet 31 of 44





Speaker



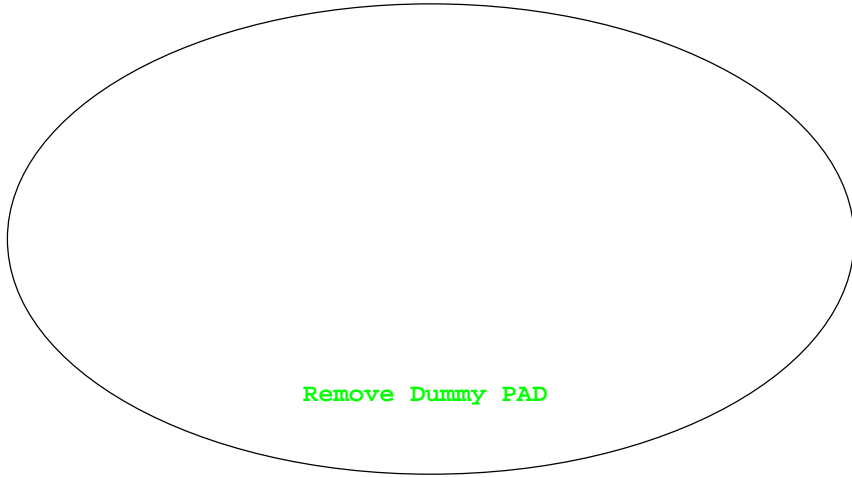
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP APA3031**

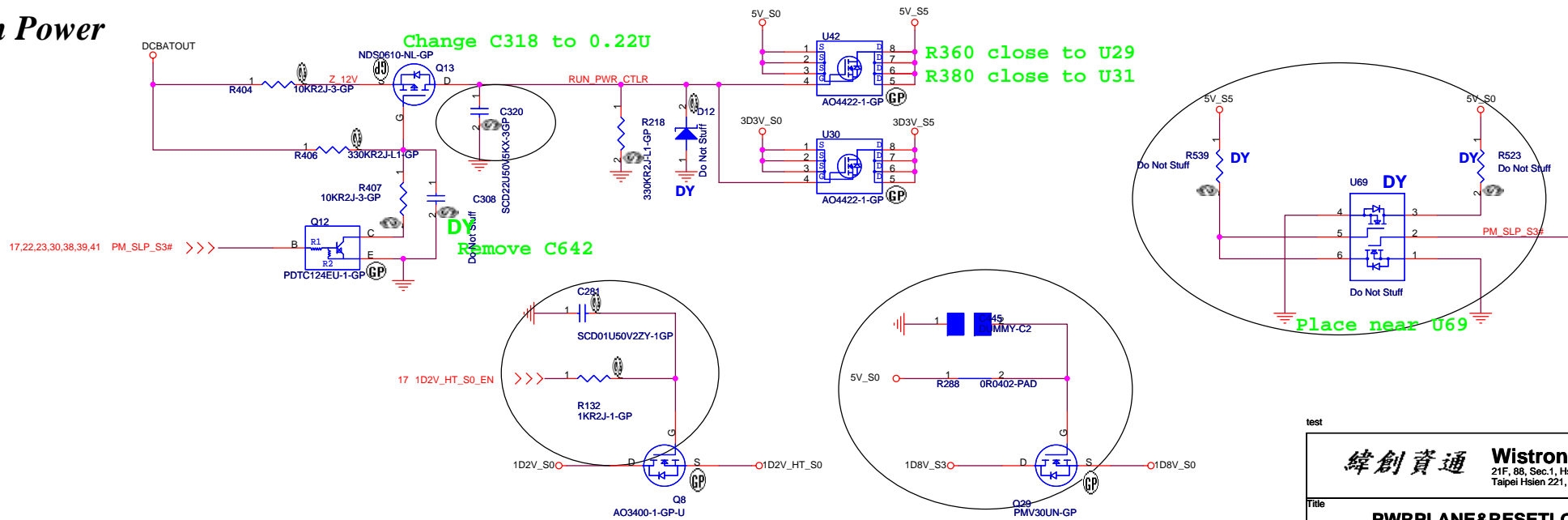
Size: A3 Document Number: **TIBET** Rev: **SA**

Date: Tuesday, August 14, 2007 Sheet 34 of 44

Suspend Power



Run Power

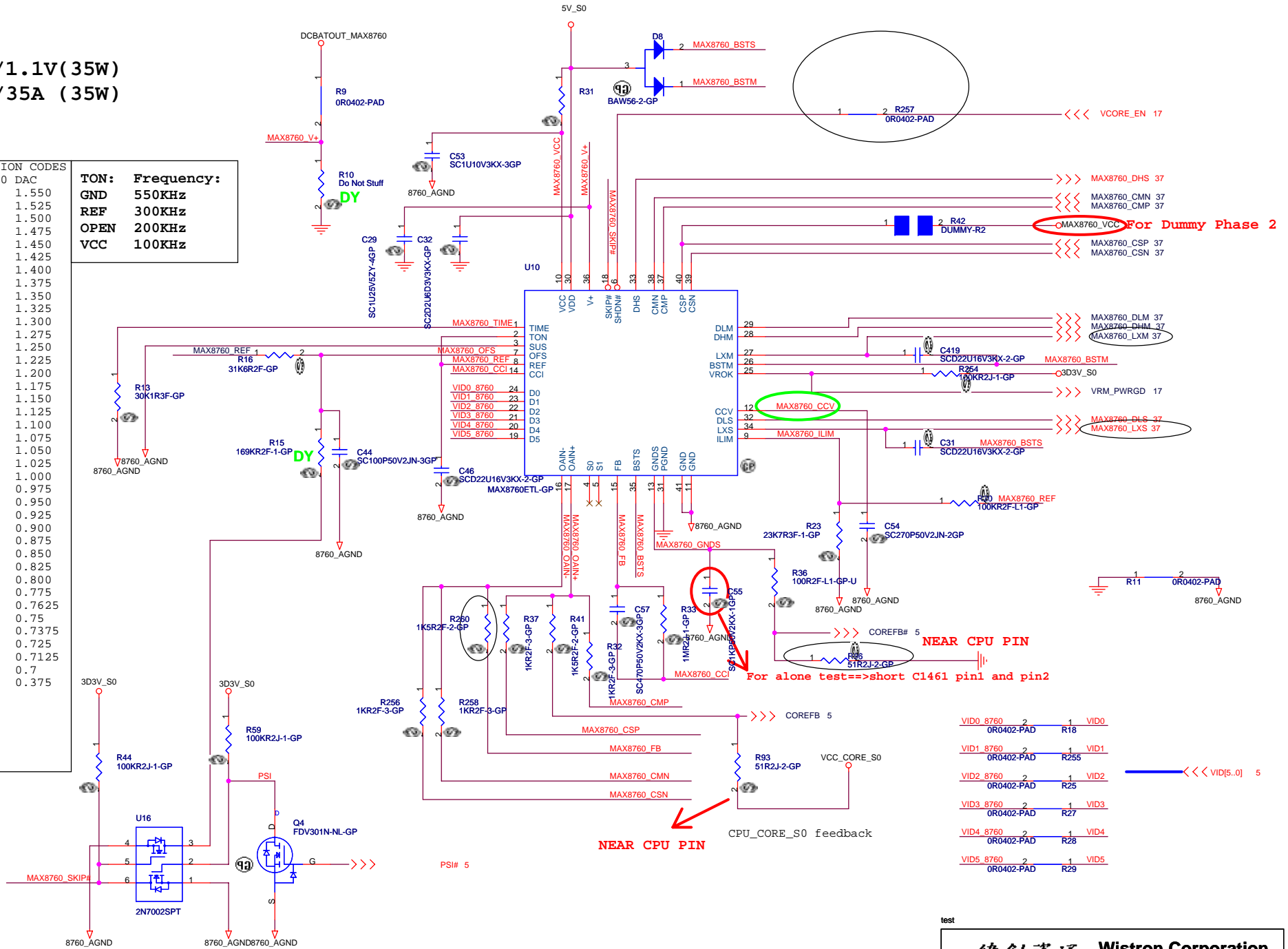


CPU_VCORE
VID=1.15V(25W)/1.1V(35W)
I_{omax}=25A(25W)/35A(35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375

TON: Frequency:
GND 550KHz
REF 300KHz
OPEN 200KHz
VCC 100KHz



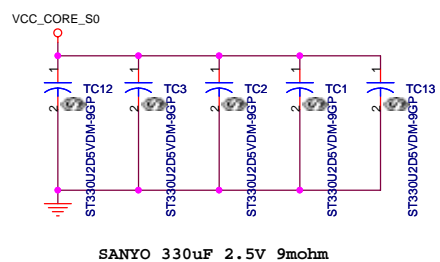
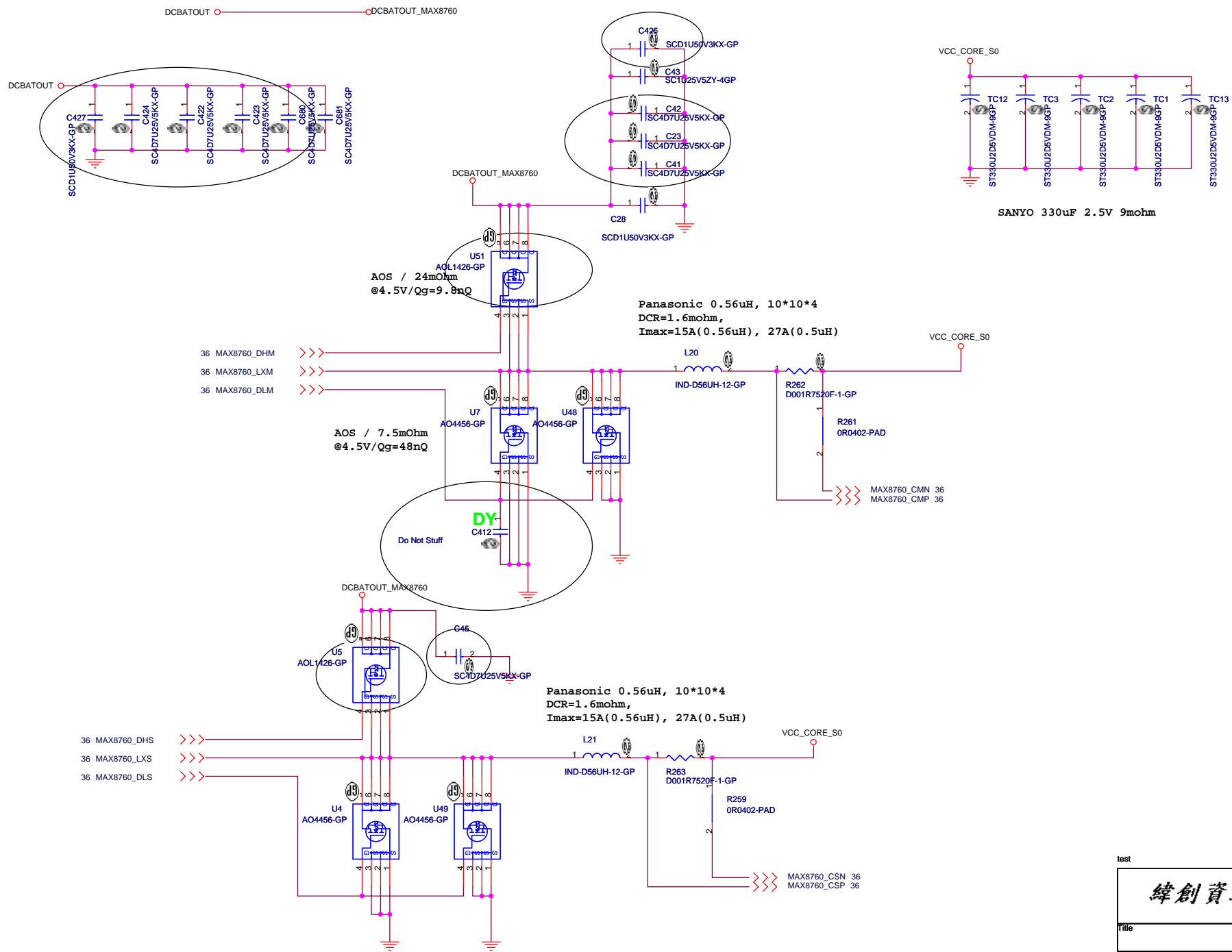
VID0 8760	2	1	VID0
OR0402-PAD		1	R18
VID1 8760	2	1	VID1
OR0402-PAD		1	R255
VID2 8760	2	1	VID2
OR0402-PAD		1	R25
VID3 8760	2	1	VID3
OR0402-PAD		1	R27
VID4 8760	2	1	VID4
OR0402-PAD		1	R28
VID5 8760	2	1	VID5
OR0402-PAD		1	R29

test

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Title: **CPU CORE MAX8760(1/2)**

Size A3	Document Number	Rev SA
TIBET		
Date: Tuesday, August 14, 2007	Sheet 36	of 44



SANYO 330uF 2.5V 9mohm

Panasonic 0.56uH, 10*10*4
DCR=1.6mohm,
Imax=15A(0.56uH), 27A(0.5uH)

AOS / 7.5mOhm
@4.5V/Qg=48nQ



Panasonic 0.56uH, 10*10*4
DCR=1.6mohm,
Imax=15A(0.56uH), 27A(0.5uH)

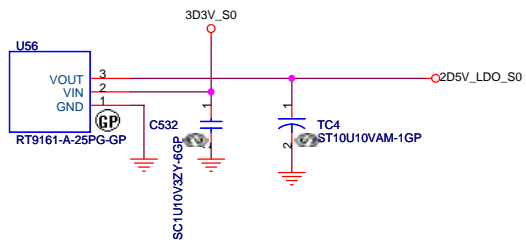
- 36 MAX8760_DHS
- 36 MAX8760_LXS
- 36 MAX8760_DLS

- MAX8760_CSN 36
- MAX8760_CSP 36

(Power Team)

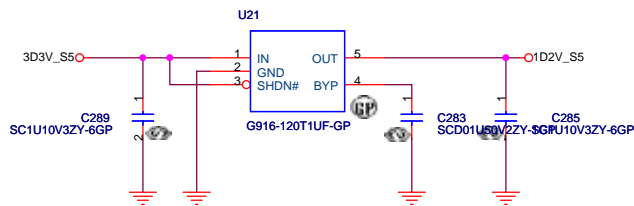
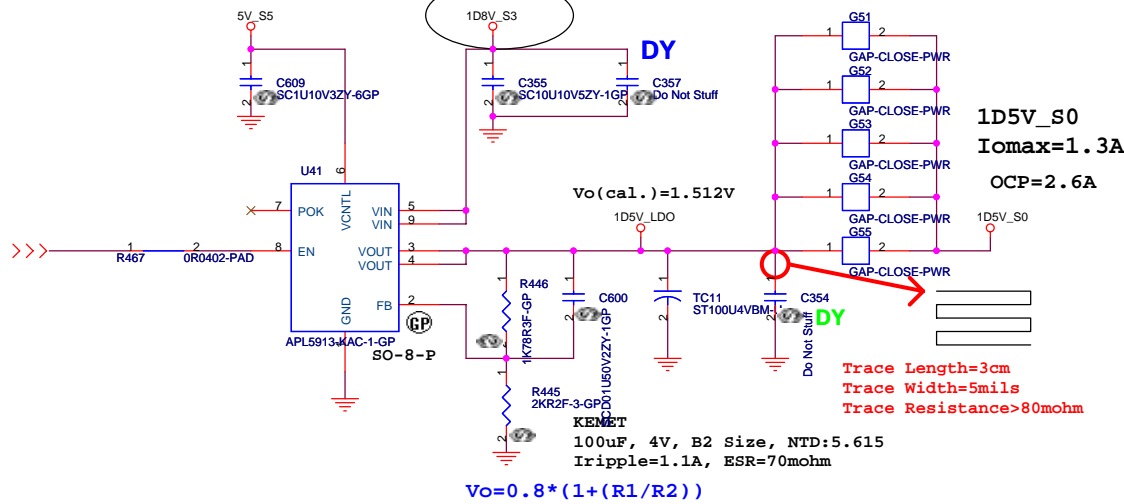
test

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CPU CORE MAX8760(2/2)	
Size A3	Document Number
TIBET	
Date: Tuesday, August 14, 2007	Sheet 37 of 44



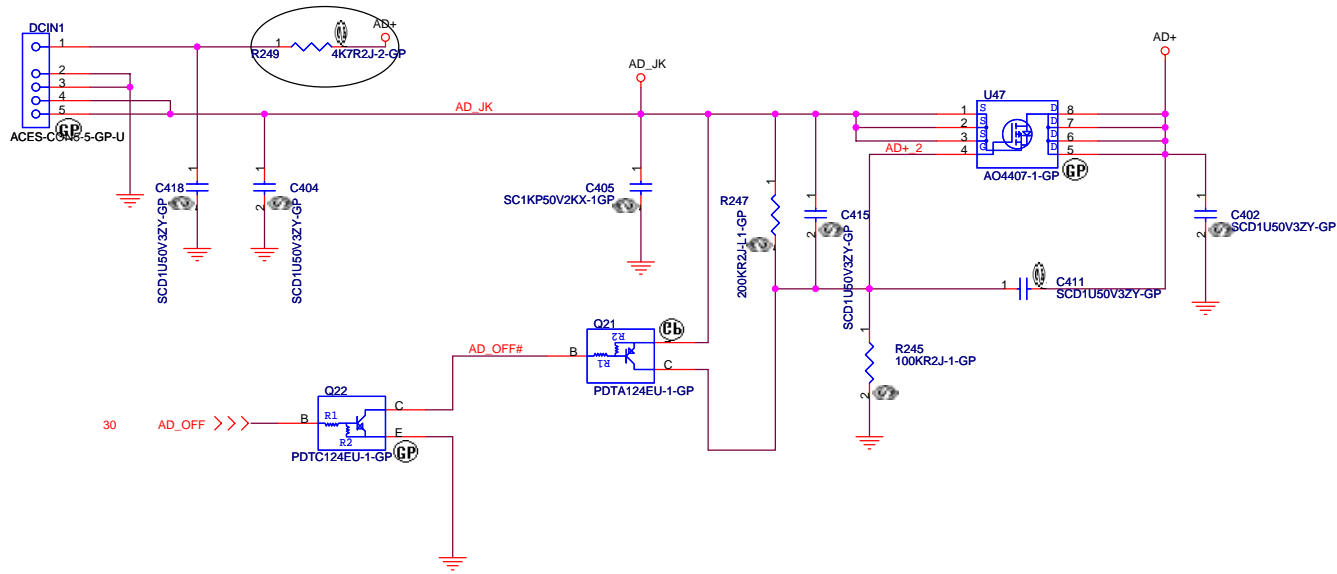
Change 3D3V_S0 to 1D8V_S3

17,22,23,30,35,38,39 PM_SLP_S3# >>>

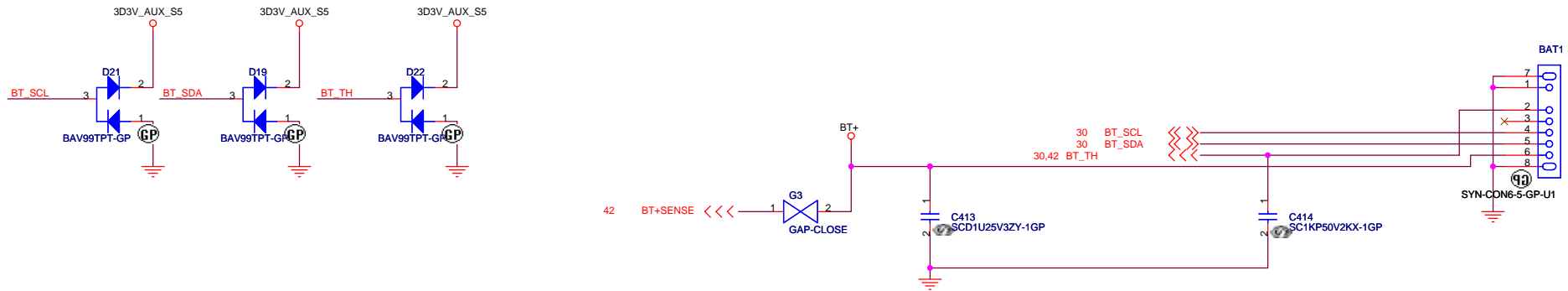


Change G914 to G916

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

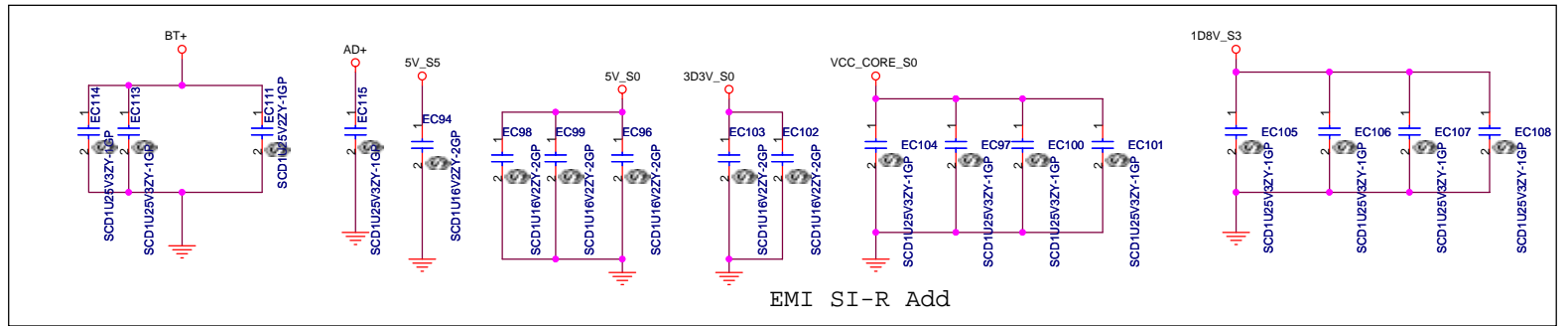
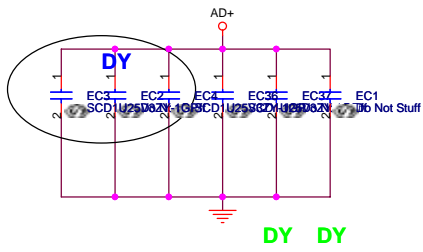


test

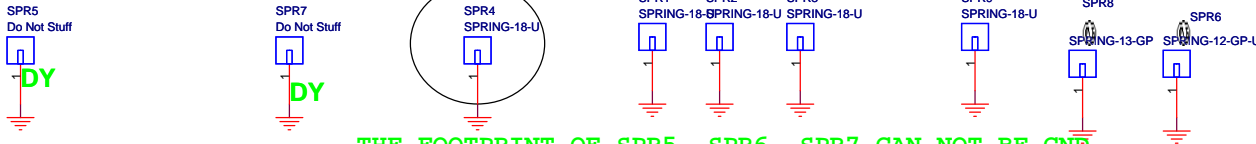
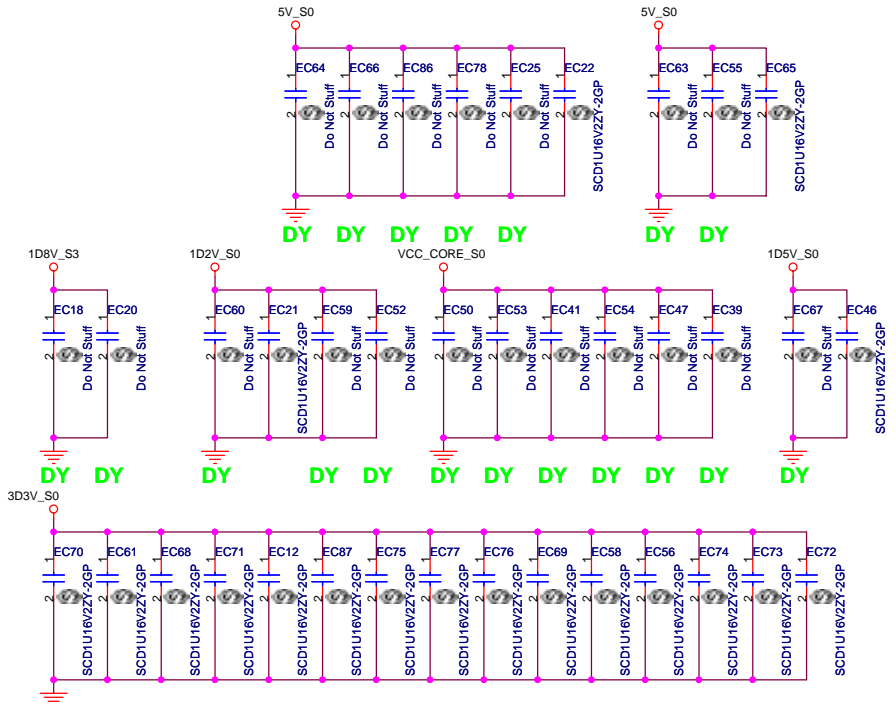
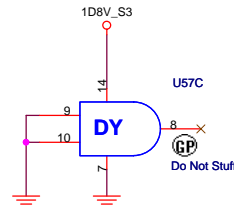
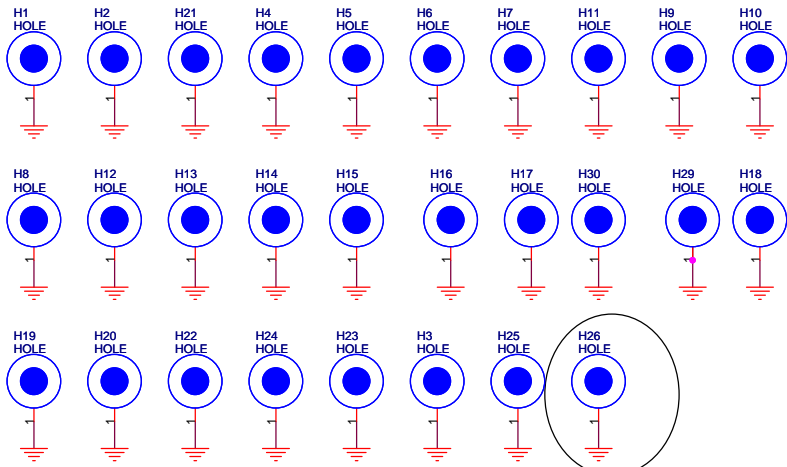
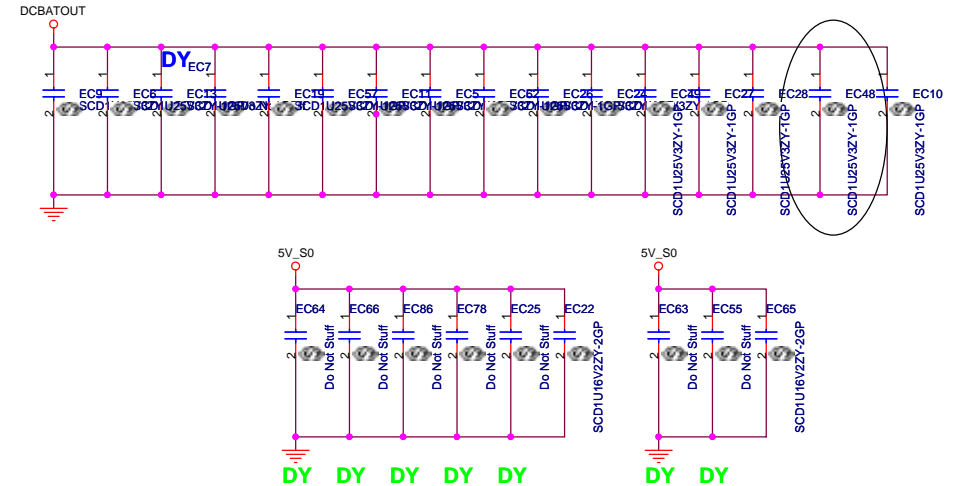
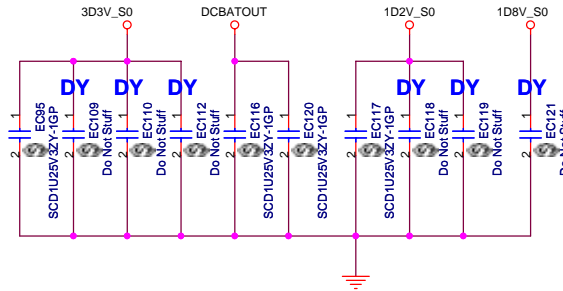
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size: A3	Document Number: TIBET	Rev: SA
Date: Tuesday, August 14, 2007	Sheet: 43	of: 44



	FF	DF
CAMERA	○	×
LAN	10/100	10/100
1394/5 IN 1	○	×
EXTRA USB	○	×
MIC	○	×
CR LED	○	×



THE FOOTPRINT OF SPR5, SPR6, SPR7 CAN NOT BE GND

test

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MISC**

Size A3 Document Number: **TIBET** Rev: **SA**

Date: Wednesday, August 15, 2007 Sheet 44 of 44